11-5865-201-30-1

TM 11-5865-201-30-1

AVIATION INTERMEDIATE MAINTENANCE MANUAL (AVIM)

COUNTERMEASURES SET AN/ALQ-156(V)1

NSN 5865-01-145-5197

RECEIVER TRANSMITTER
A7
XA7
J1
12
47
11
19
10
14
43
42
36
48
RG1 ALARM L
ECM1L
RG2 ALARM L
LSDLL
RG3
MI
EC
RCVG. DOPP PROC AND INTFR MON CKTS
OPRT
OPRT1
OPRT 7 FRO
MING CKTS
J2
J1
6
23
4
MUX
SET
M3L
OM
TFR

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RECEIVER TRANSMITTER DISASSEMBLY 3-43
CONTROL INDICATOR CHECK PROCEDURE 4-1

HEADQUARTERS, DEPARTMENT OF THE ARMY

MARCH 1984

D 101.11:

FIRST AID

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER
3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL
4. SEND FOR HELP AS SOON AS POSSIBLE
5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

TECHNICAL MANUAL

NO. 11-5865-201-30-1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 5 March 1984

AVIATION INTERMEDIATE MAINTENANCE MANUAL (AVIM) FOR COUNTERMEASURES SETS AN/ALQ-156 (V)1 NSN 5865-01-145-5197

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703.

In either case, a reply will be furnished direct to you.

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HOW TO USE THIS MANUAL

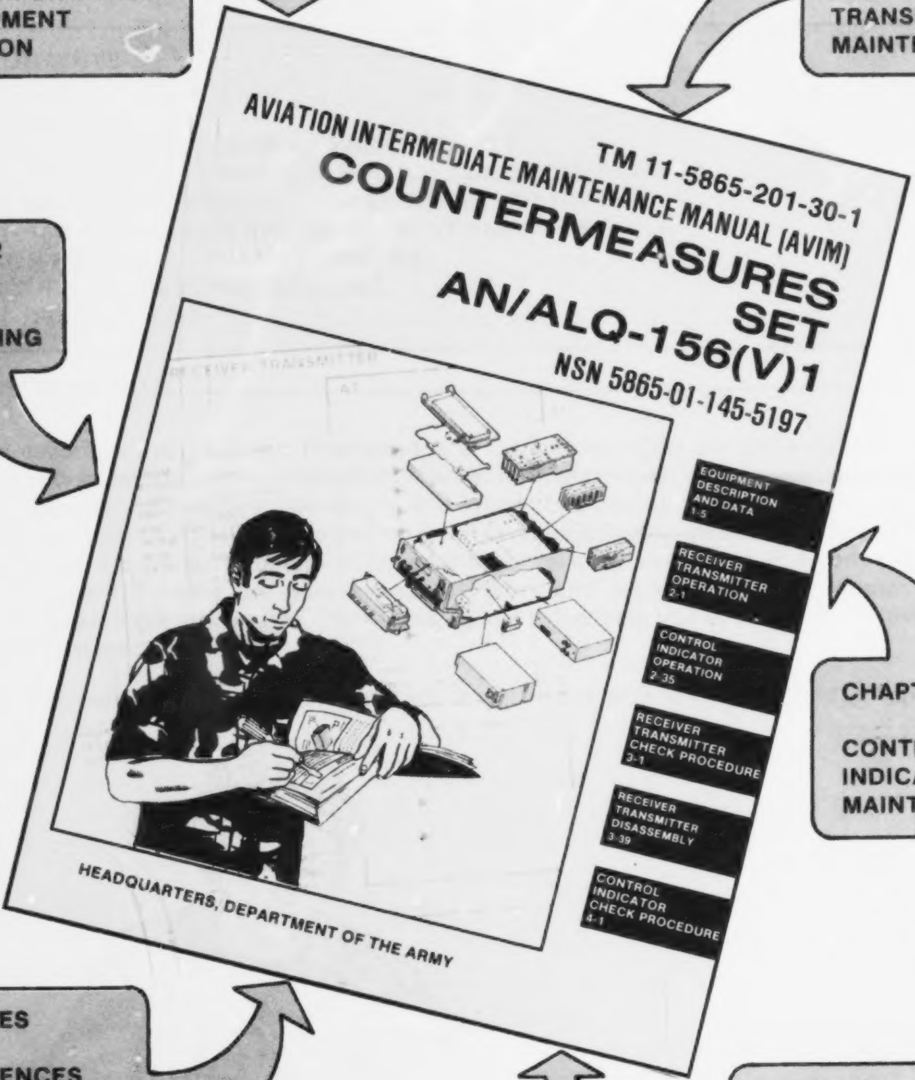
Before your attempt to maintain the Countermeasures Set AN/ALQ-156(V)1 it is important to familiarize yourself with this manual. Each of the four chapters is unique, and you will save time if you know where to go for the information you need. Briefly, this is how the manual is organized.

CHAPTER 1

GENERAL INFORMATION AND EQUIPMENT DESCRIPTION

CHAPTER 2

SYSTEM FUNCTIONING



TM 11-5865-201-30-1

AVIATION INTERMEDIATE MAINTENANCE MANUAL (AVIM)

COUNTERMEASURES SET

AN/ALQ-156(V)1

NSN 5865-01-145-5197

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HEADQUARTERS, DEPARTMENT OF THE ARMY

CHAPTER 3

RECEIVER TRANSMITTER MAINTENANCE

CHAPTER 4

CONTROL INDICATOR MAINTENANCE

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- **B. EXPENDABLE SUPPLIES AND MATERIALS LIST**

APPENDICES

- **C. NONSTANDARD ABBREVIATIONS**

GLOSSARY

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1-1. SCOPE OF MANUAL

This manual describes operation and maintenance of Countermeasures Set AN/ALQ-156(V)1 at the Aviation Intermediate Maintenance (AVIM) level. This introductory chapter contains general information, (this section), description and data (Section II), and system functioning (Section III). The information contained in Sections II and III will enable you to identify system subassemblies and understand system operation. Chapter 2 presents a functional description of receiver transmitter and control indicator operation. Chapters 3 and 4 are maintenance chapters and contain test, troubleshooting, and subassembly replacement procedures. These procedures will enable you to keep the equipment in a state of operational readiness.

Other related manuals which you will need and which will be available to you are listed in Appendix A.

1-2. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System (TAMMS).

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73A/AFR 400-54/MCO 4430.3F.

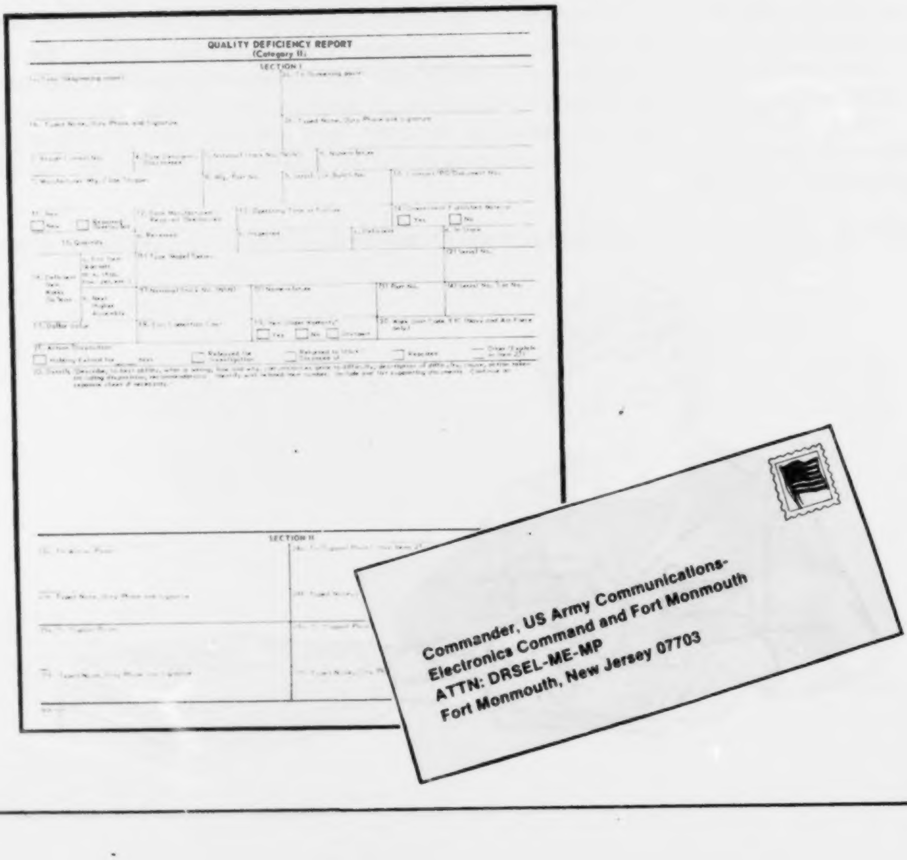
c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-3. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

1-4. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)

If your countermeasures set needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703. We'll send you a reply.



QUALITY DEFICIENCY REPORT
(Category II)

SECTION I

SECTION II

Commander, US Army Communications-
Electronics Command and Fort Monmouth
ATTN: DRSEL-ME-MP
Fort Monmouth, New Jersey 07703

1-5. DESTRUCTION OF ARMY MATERIEL TO PREVENT ENEMY USE

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

1-6. PREPARATION FOR STORAGE AND SHIPMENT

Instructions for preparations for storage and shipment including administrative storage are given in Chapter 3, Section VI, of TM 11-5865-201-12.

1-7. NOMENCLATURE CROSS REFERENCE LIST

The following common names and abbreviations are used in this manual for simplicity.

OFFICIAL NOMENCLATURE	COMMON NAME	ABBREVIATION
Countermeasures Set AN/ALQ-156(V)1	Countermeasures Set	CM Set
Receiver Transmitter RT-1220/ALQ-156(V)	Receiver Transmitter	RT
Control Indicator C-10131/ALQ-156(V)	Control Indicator	CI
Antenna AS-3149/ALQ-156(V)	Antenna	(None)
Frequency Multiplier Oscillator	(None)	FMO
Test Set, Countermeasures TS-3609/ALQ-156(V)	TS-3609	(None)
Test Set, Countermeasures Set Assembly (Part of TS-3609)	Test Set	TS
Fan, Tubeaxial	Blower	(None)

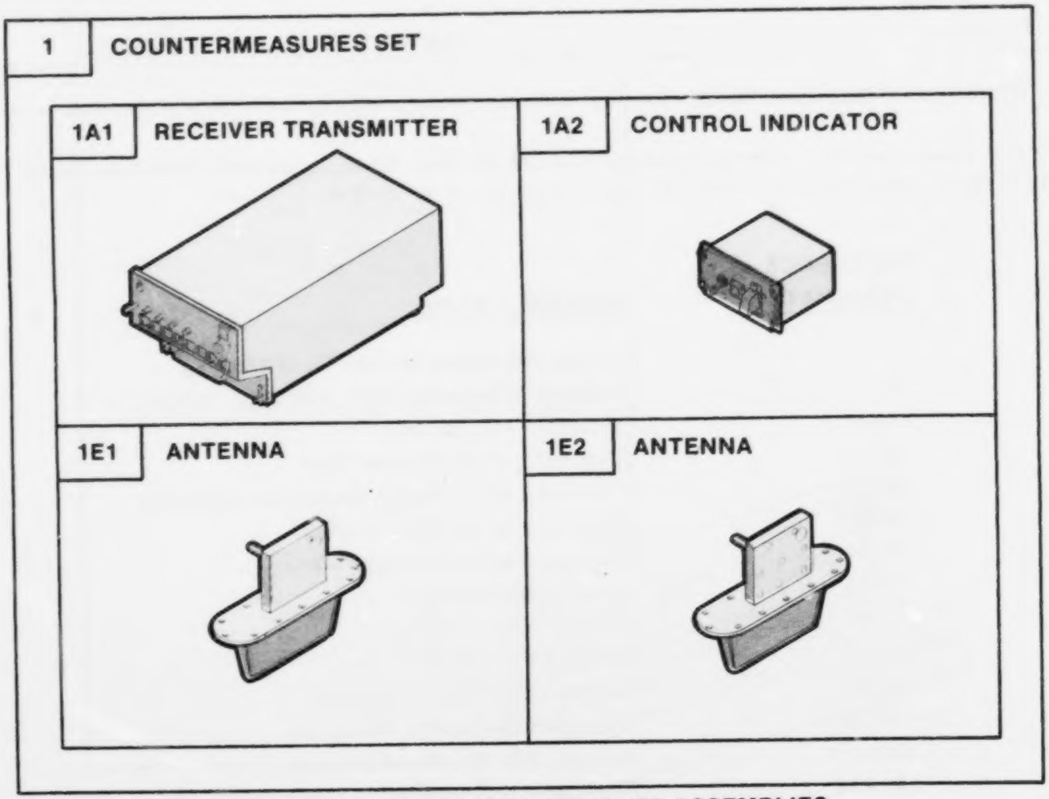
1-8. REFERENCE DESIGNATORS

The major assemblies and subassemblies of the CM set have an assigned reference designator. The names of these units and their reference designators are given below.

REFERENCE DESIGNATOR	ASSEMBLY NAME
1	Countermeasures Set, AN/ALQ-156(V)1
1A1	Receiver Transmitter, RT-1220/ALQ-156(V)
1A1A1	Channel 1 Range Gate
1A1A2	Channel 1 Mixer/Clutter Filter
1A1A3	Channel 2 and 3 Range Gate Card Assembly
1A1A4	Channel 2 Mixer/Clutter Filter
1A1A5	Channel 3 Mixer/Clutter Filter
1A1A6	Sync Digital Interface
1A1A7	Synchronizer Timing
1A1A8	Synchronizer BITE
1A1A9	Synchronizer Microprocessor
1A1A10	Reference Generator Multiplier
1A1A11	Accumulator/Envelope Detector
1A1A12	Post Detection Integrator/Blade Rejection

1-8. REFERENCE DESIGNATORS (Continued)

1A1A13	Deltic Memory Control
1A1A14	Circuit Card Assembly
1A1A15	Duplexer
1A1A16	First IF Amplifier
1A1A17	Directional Coupler
1A1A18	Power Divider
1A1A19	CM Heat Assembly
1A1AR1	Power Amplifier
1A1AT1	Attenuator
1A1B1	Fan
1A1ET1	Elapsed Time Indicator
1A1PS1	Power Supply
1A1Y1	Frequency Mutiplier Oscillator
1A2	Control Indicator, C-10131/ALQ-156(V)
1A2A1	Control Indicator Card Assembly
1E1	Antenna, AS-3149/ALQ-156(V)
1E2	Antenna, AS-3149/ALQ-156(V)


1
COUNTERMEASURES SET
1A1
RECEIVER TRANSMITTER
1A2
CONTROL INDICATOR
1E1
ANTENNA
1E2
ANTENNA

REFERENCE DESIGNATORS OF MAJOR ASSEMBLIES

SECTION II. EQUIPMENT DESCRIPTION AND DATA

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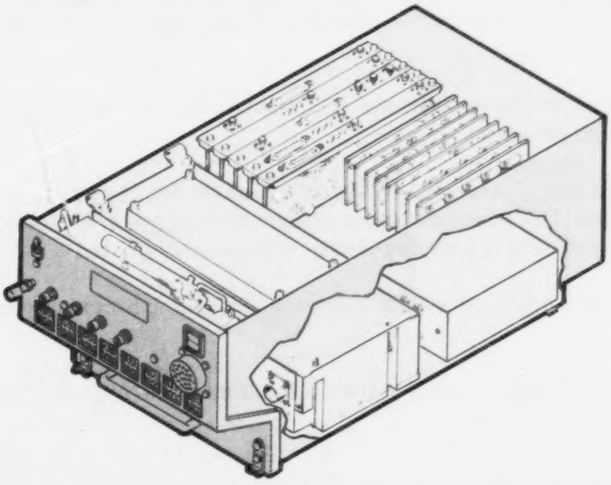
1-9. GENERAL

A brief description and principles of operation for the AN/ALQ-156(V)1 Countermeasures Set are given in TM 11-5865-201-12. This section will provide you with descriptions of the components of the RT and CI which you may have to replace during maintenance of the system.

1-10. LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS

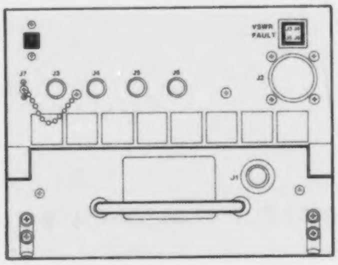
The following pages illustrate and describe briefly the major components of the receiver transmitter. Refer to TM 11-5865-201-12 for additional information for the exterior mounted devices.



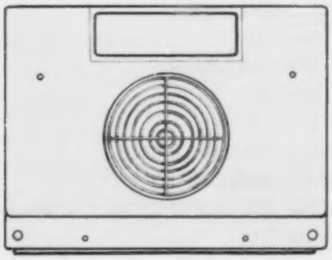
LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS (Continued)

EXTERIOR

The receiver transceiver cover provides protection against damage and contamination for its major components. Constructed of aluminum and enclosing four sides and rear end, it also provides EMI (electromagnetic interference) protection for the receiver transmitter. Note that the front of the receiver transmitter has the electrical connectors, elapsed time indicator, VSWR fault indicators, and eight air input slots. The fan is mounted on the rear end and exhausts heated air through a circular opening in the cover. Circuit card assembly, A19, the CM preheat assembly is mounted on the inside of the fan housing.



FRONT



REAR

INTERIOR

With the cover removed, you can locate most of the assemblies of the RT. The second IF, synchronizer circuit cards, and doppler processor circuit cards are located at the rear of the chassis. The five second IF cards are located on the left side and are larger than the logic cards located in the card cage at the right.

The duplexer is mounted at the front of the RT chassis. Its four antenna output jacks protrude through holes in the front panel. .

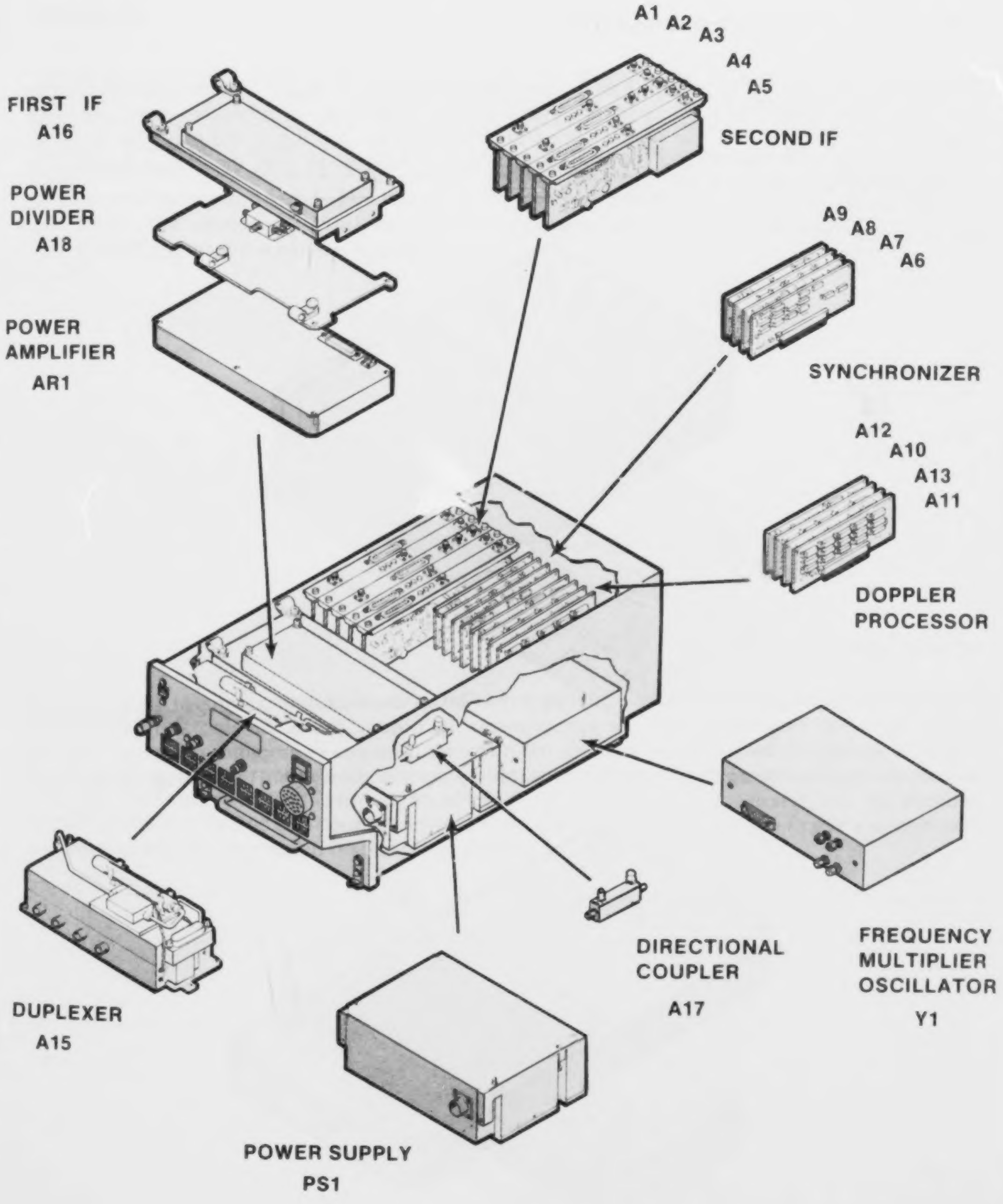
Behind the duplexer the first IF assembly rests on a bracket which is supported by standoff posts securing a mounting plate. The power divider is attached to this plate. The power amplifier is located beneath the mounting plate and is also secured by the standoff posts.

A directional coupler is mounted to the right edge of the mounting bracket which supports the first IF assembly.

The power supply and FMO are mounted in the bottom half of the chassis. The FMO, located in the rear, is supported by shock mounts.

LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS (Continued)

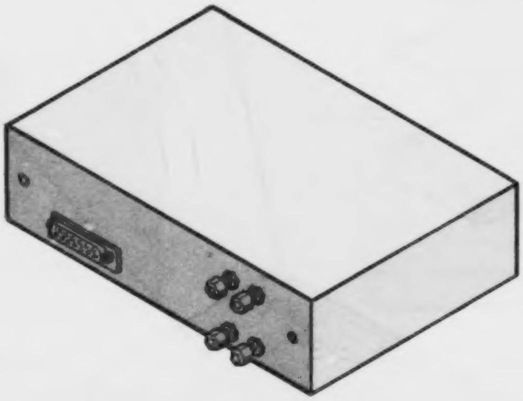
INTERIOR (Continued)


A1 A2 A3 A4 A5
SECOND IF
FIRST IF
A16
POWER DIVIDER
A18
POWER AMPLIFIER
AR1
A9 A8 A7 A6
SYNCHRONIZER
A12 A10 A13 A11
DOPPLER PROCESSOR
DUPLEXER
A15
DIRECTIONAL COUPLER
A17
FREQUENCY MULTIPLIER OSCILLATOR
Y1
POWER SUPPLY
PS1

LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS (Continued)

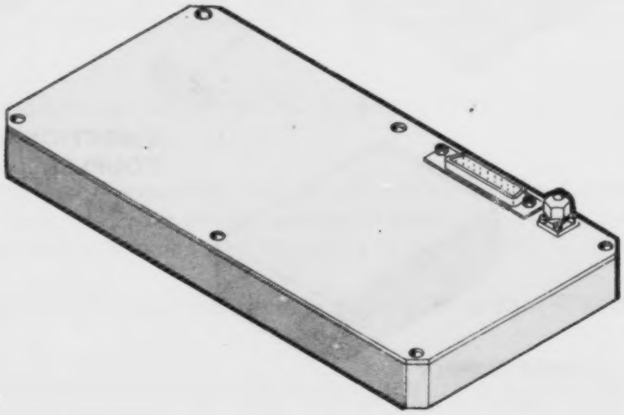
FREQUENCY MULTIPLIER OSCILLATOR

The frequency multiplier oscillator (FMO) generates the precise RF and IF frequencies required by the CM set. Also, all system timing signals are derived from a 5 MHz signal generated within the FMO. The basic oscillator within this unit is temperature-controlled in order to maintain the required frequency stability. When the CM set is operated in the preheat mode, only the heater maintaining this temperature control is energized.



POWER AMPLIFIER

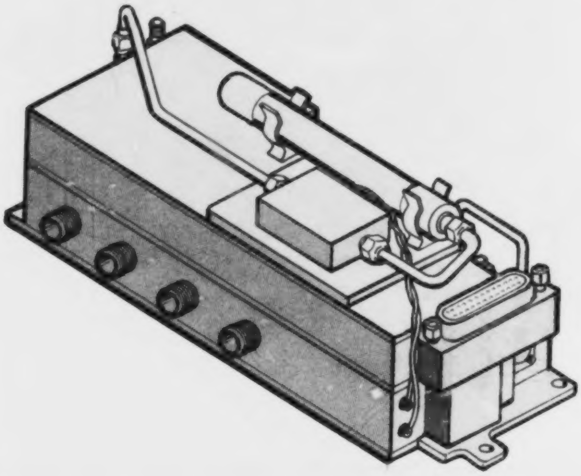
The power amplifier receives the RF signal from the FMO and a modulating signal at the system PRF (pulse repetition frequency) from the synchronizer. Its output, the modulated and amplified RF signal, is applied to the antennas through the duplexer. The power amplifier contains a thermal switch which will cause system shutdown if the internal temperature within this unit exceeds normal limits.



LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS (Continued)

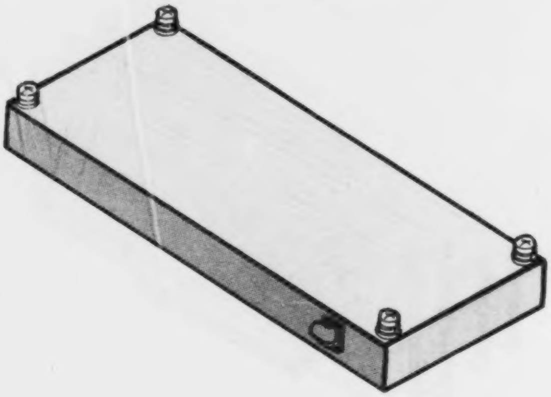
DUPLEXER

The duplexer is essentially an RF switch which directs RF energy to or from the two antennas. An internal RF circulator connects the power amplifier output to the switch during the transmit mode and connects an RF preamplifier to the switch during the receive mode. During operation, the duplexer sends out a series of RF pulses to one antenna and receives radar return energy (target echos) between transmissions. After a preset interval, the switch connects to the second antenna and again transmits and receives for this same interval. This action continues whenever the CM set is operating. The duplexer also contains sensing devices which will initiate BITE (built in test equipment) alarms if the system malfunctions.



FIRST IF ASSEMBLY

The first IF assembly receives RF energy (radar return) from the duplexer during the receive intervals. This energy is divided into an inner and outer channel within the first IF, and the signal in each channel is amplified and double converted into the first IF frequency. The first IF also contains an interference detector which reacts to large signal returns.

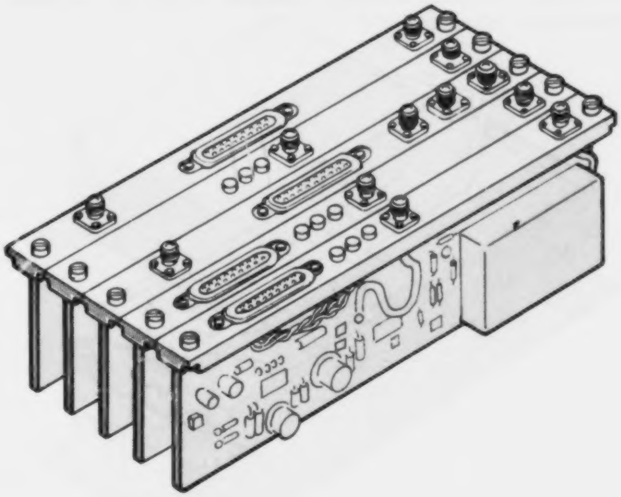


LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS (Continued)

SECOND IF ASSEMBLY

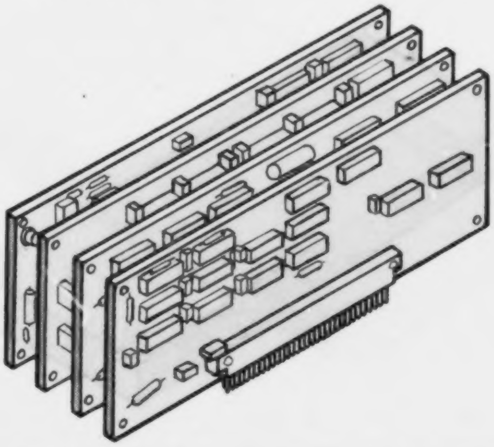
The second IF assembly consists of circuit card assemblies A1 through A5. The inner channel IF signal from the first IF is range-gated (RG1) in the A1 card, and converted and filtered in the A2 card. The outer channel IF signal from the first IF is divided in the A3 card and applied to two range gates (RG2 and RG3). The A4 card provides conversion and filtering for the RG2 signal, while the A5 card provides conversion and filtering for the RG3 signal.

The A2, A4, and A5 cards also contain ECM (electronic countermeasures) interference detectors. The A3 card contains a mutual interference (MI) detector.



SYNCHRONIZER

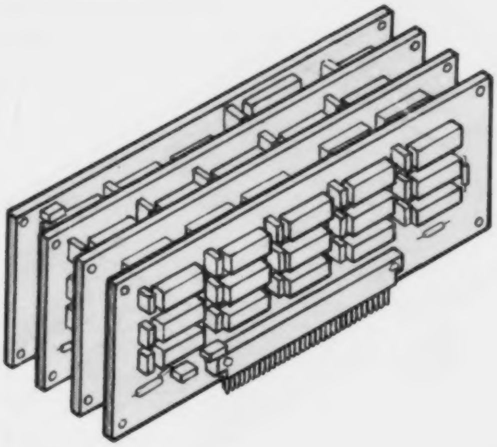
The synchronizer consists of circuit cards A6 through A9. The synchronizer generates all system timing signals from the 5 MHz FMO output, contains the BITE (built-in-test-equipment) circuits, the microprocessor circuits and the interface circuits for use with the test set during testing. The microprocessor circuits accept the alarm, interference, and control signals, and output system commands in accordance with the program stored in memory.



LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS (Continued)

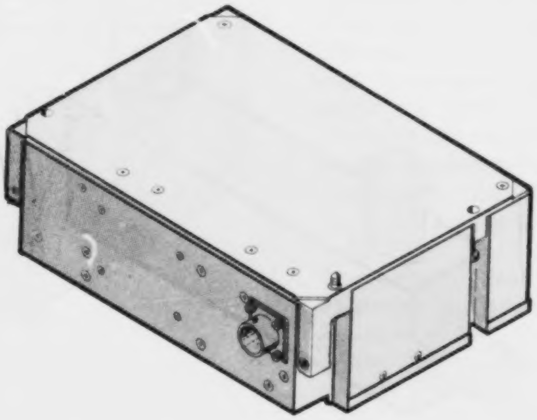
DOPPLER PROCESSOR

The doppler processor consists of circuit card assemblies A10 through A13. The doppler information contained in the range-gated data signals from the second IF is filtered into discrete doppler channels, and is stored and added over each processing period. If the summed outputs in any range gated interval exceeds a preset threshold, the doppler processor produces a range-gated alarm. This is sent to the microprocessor circuits in the synchronizer for further processing.



POWER SUPPLY

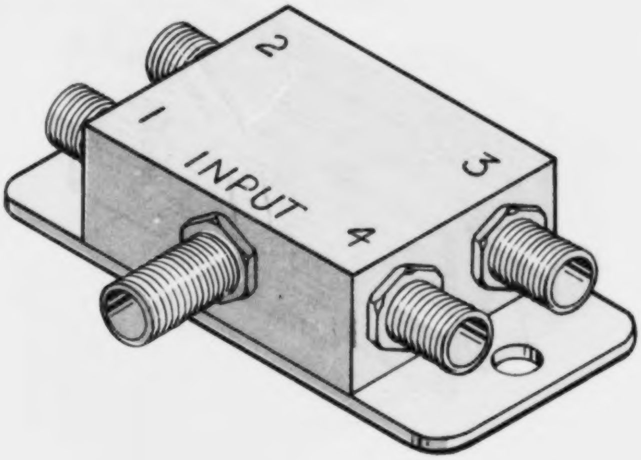
The power supply converts the 115 V, 3-phase, 400 Hz input power from the aircraft power bus into eight dc voltage required for system operation. The conversion is made through the use of an inverter synchronized to system timing. The power supply also contains self-monitor circuits to prevent system operation when an overvoltage or overcurrent condition exists.



LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS (Continued)

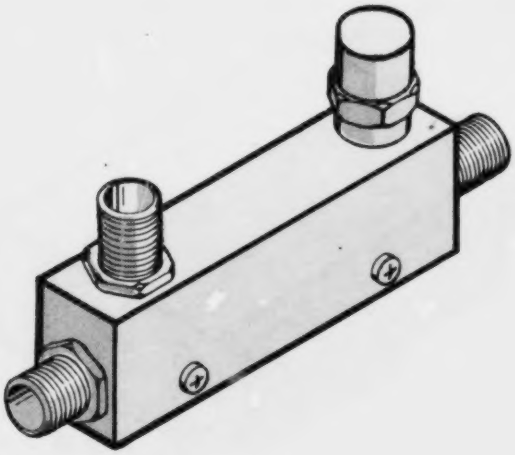
POWER DIVIDER

The power divider receives a 5 MHz input from the FMO. It has four, 5 MHz outputs three of which are applied as local oscillator signals to the mixer stages in the second IF assembly for conversion of the second IF signal to video. The fourth 5 MHz signal is applied to a mixer used with the mutual interference detector located on the second IF A3 card assembly.



DIRECTIONAL COUPLER

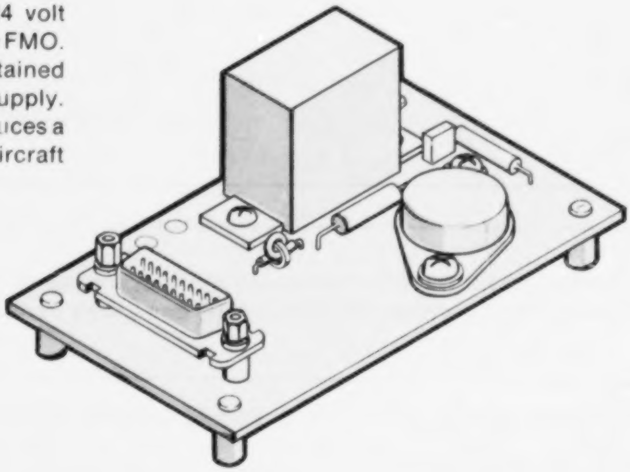
The directional coupler receives the F0 signal from the FMO and routes this signal to the power amplifier. The 30 dB port of the coupler is connected to the front panel connector J7. This small part of the F0 signal is applied to the test set for generation of a drive signal. F0 may also be monitored at connector J7.



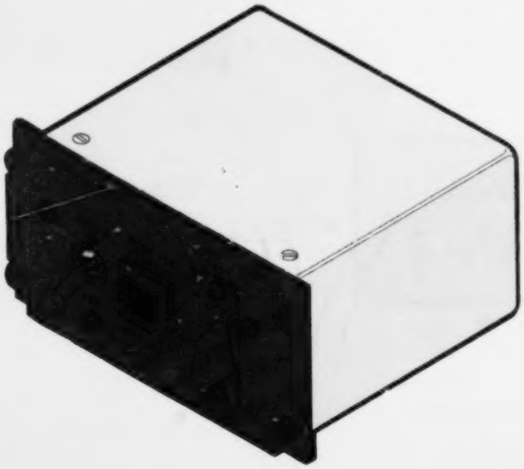
LOCATION AND DESCRIPTION OF MAJOR RECEIVER TRANSMITTER COMPONENTS (Continued)

CM PREHEAT CARD ASSEMBLY

The CM preheat card controls the +24 volt power applied to the crystal heater in the FMO. In normal operation this power is obtained from the +24 volt section of the power supply. With the system turned off, this unit produces a +24 volt output for the heater when the aircraft CM preheat switch is actuated.



1-11. LOCATION AND DESCRIPTION OF MAJOR CONTROL INDICATOR COMPONENTS



CONTROL INDICATOR

The control indicator, as the name implies, provides the operator with control of the CM set and indications of its operation. The POWER switch turns the set on and the PUSH FOR STANDBY switch places it in a standby mode. The dual STATUS indicator informs the operator when the system is in standby mode and if warmup has been achieved. Relays, within the control indicator, actuate the CM JAM and CM INOP indicators on the aircraft's master caution panel (not part of the CM set). The FLARE TEST switch is used only to test the M-130 flare dispenser system.

The control indicator contains one circuit card assembly. Front panel lighting is provided by a replaceable edge-lit panel whose brightness is controlled by the aircraft cockpit lighting system.

1-12. EQUIPMENT DATA

Refer to TM 11-5865-201-12 for unclassified physical and electrical data for the countermeasures set. For classified performance data, refer to TM 11-5865-201-30-2.

SECTION III.
SYSTEM FUNCTIONING

SECTION CONTENTS **PAGE**

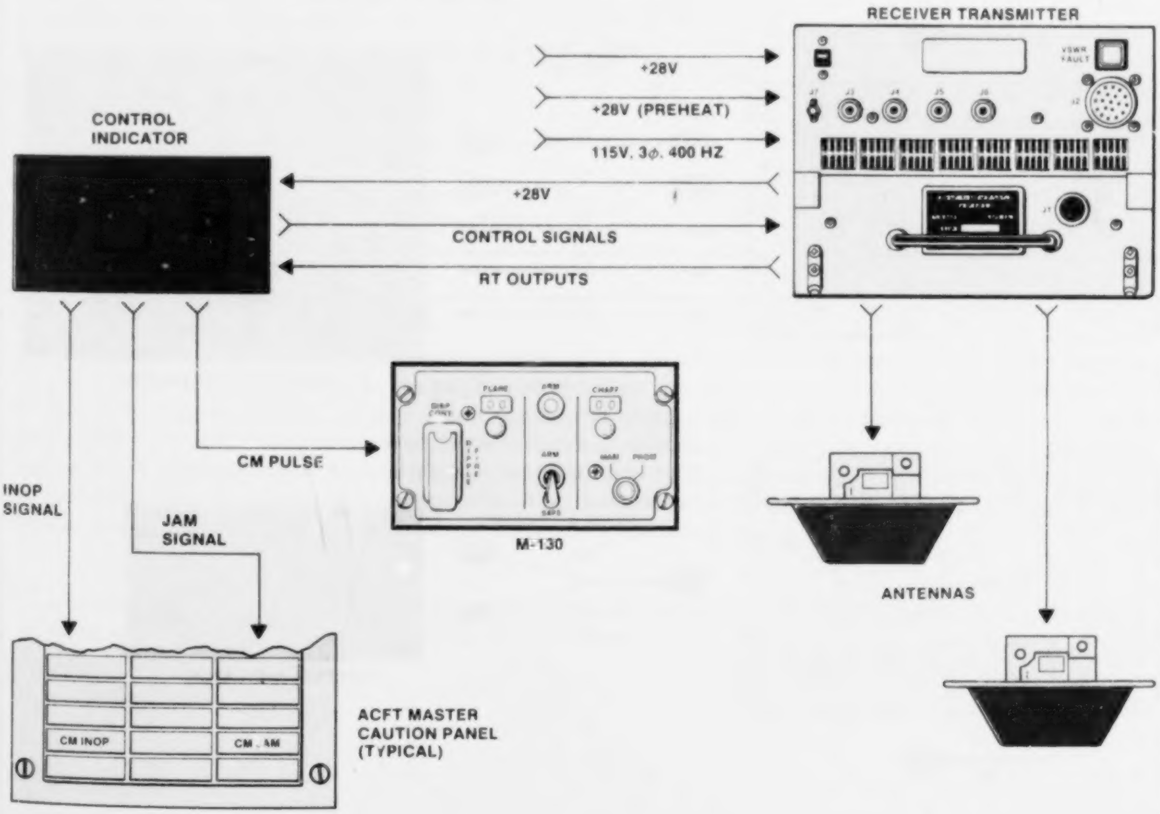
GENERAL 1-15
FUNCTIONAL OPERATION OF COUNTERMEASURE SET 1-15
BENCH TEST OPERATION 1-16

1-13. GENERAL

This section describes the operation of the CM set as installed in the aircraft. It also relates operation to bench testing procedures which you will use to check and fault-isolate the receiver transmitter and control indicator.

1-14. FUNCTIONAL OPERATION OF COUNTERMEASURES SET

A simplified block diagram of the CM set is shown below. Aircraft 115 V ac and +28 V power are connected to the receiver transmitter via aircraft cabling. The 115 V ac is the primary power source for the system while the +28 V is used for system control only.


RECEIVER TRANSMITTER
+28V
+28V (PREHEAT)
115V, 3φ, 400 HZ
CONTROL INDICATOR
+28V
CONTROL SIGNALS
RT OUTPUTS
CM PULSE
M-130
INOP SIGNAL
JAM SIGNAL
ANTENNAS
CM INOP
CM JAM
ACFT MASTER CAUTION PANEL (TYPICAL)

1-14. FUNCTIONAL OPERATION OF COUNTERMEASURES SET (Continued)

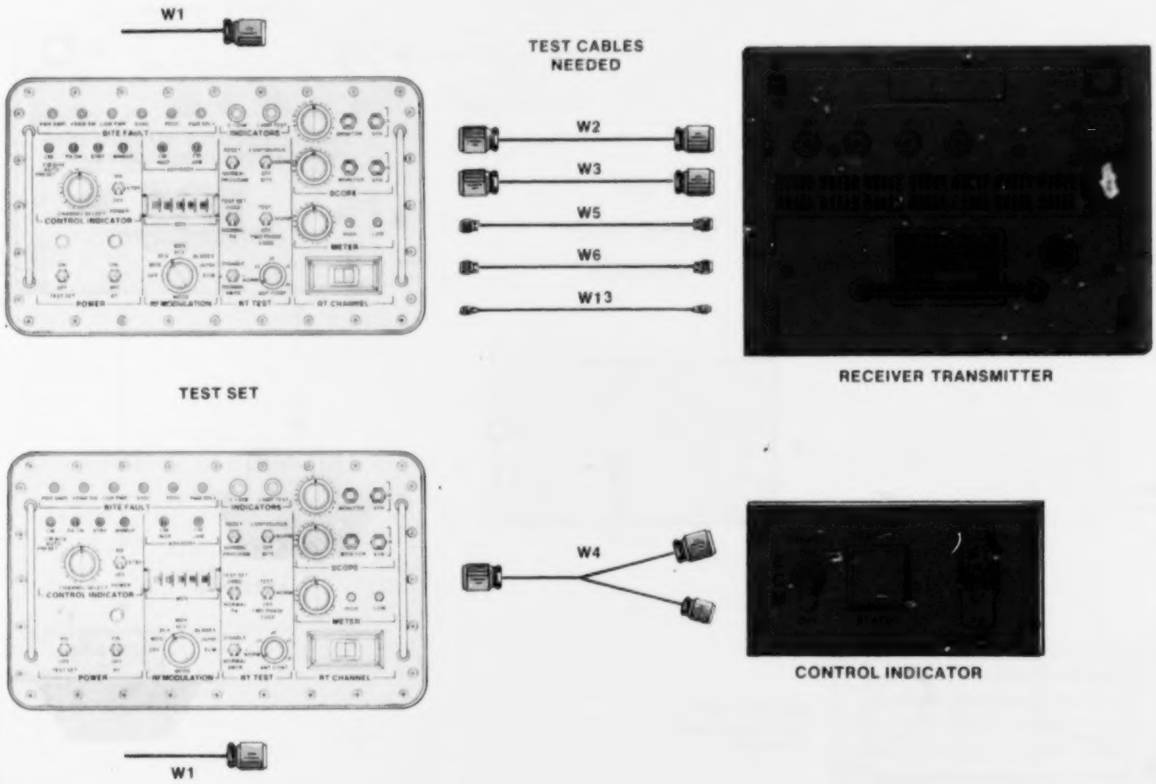
The control indicator receives the +28 V dc from the receiver transmitter. When the POWER switch is set to ON, this voltage is returned to the receiver transmitter as a control signal to energize it. The WRMUPL signal from the receiver transmitter causes the WRMUP indicator to go out indicating to the operator that FMO warmup is completed. The STBY signal to the receiver transmitter places it in a standby mode where all circuits are energized except the transmitting circuits.

If the +28 V dc (preheat) power is supplied to the receiver transmitter in advance of operation, the normal warmup period is greatly reduced.

The two antennas are driven by the power amplifier during transmit mode and receive reflected energy from targets during the receive mode. If a real target exists, the receiver transmitter outputs a CM pulse command to the M-130 system via the control indicator. If jamming is detected or the CM set becomes inoperative, the receiver transmitter outputs jam or inop signals to the control indicator which relays them to indicators on the aircraft master caution panel. This alerts the pilot to the presence of these conditions.

1-15. BENCH TEST OPERATION

During bench testing, you may test the receiver transmitter or control indicator individually, not as a system. The test set provides all interfaces needed to operate and test either unit including power input, load, control, and simulated test signals. The test cables required for bench test are supplied with the Countermeasures Test Set TS-3609/ALQ-156(V).



CHAPTER 2
FUNCTIONAL OPERATION

SECTION I.
RECEIVER TRANSMITTER OPERATION

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2-1. GENERAL DESCRIPTION

A brief description of the assemblies within the receiver transmitter and their purpose was presented to you in Section II of Chapter 1. In the pages which follow, the operation of the RT will be described in terms of functional circuit groups. Each functional circuit will relate to portions of one or more assemblies of the RT. An overview of these functional circuits and their interrelationships is shown in figure 2-1. A detailed description and a functional schematic diagram for each functional circuit will be presented to you in subsequent paragraphs. Also, functional schematics and descriptions for the RT power distribution functions (not shown in figure 2-1) are provided.

The mnemonic codes used in the functional descriptions and functional schematic diagrams are defined in Appendix C, Glossary of Nonstandard Abbreviations.

2-1. GENERAL DESCRIPTION (Continued)

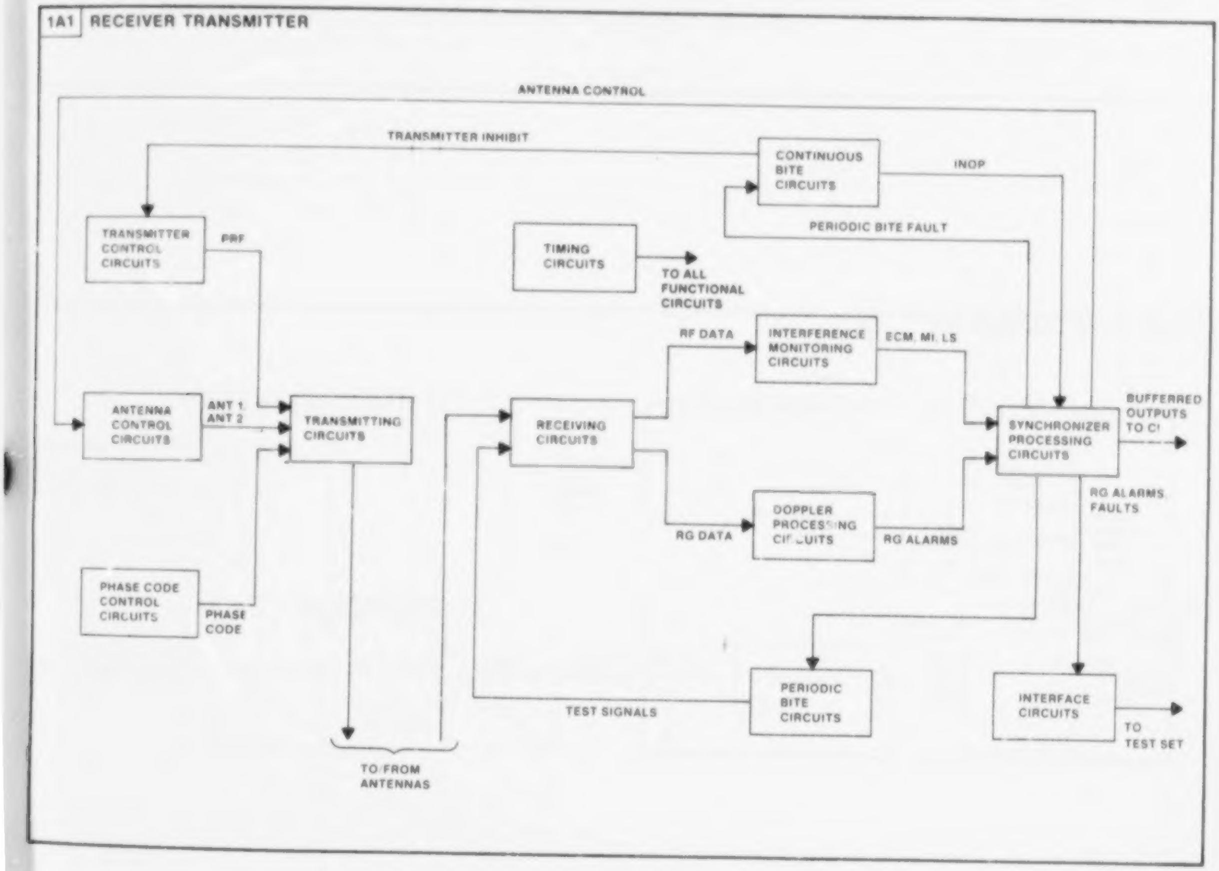

1A1
RECEIVER TRANSMITTER
ANTENNA CONTROL
TRANSMITTER INHIBIT
CONTINUOUS BITE CIRCUITS
INOP
TRANSMITTER CONTROL CIRCUITS
PRF
TIMING CIRCUITS
TO ALL FUNCTIONAL CIRCUITS
PERIODIC BITE FAULT
RF DATA
INTERFERENCE MONITORING CIRCUITS
ECM, MI, LS
ANTENNA CONTROL CIRCUITS
ANT 1
ANT 2
TRANSMITTING CIRCUITS
RECEIVING CIRCUITS
SYNCHRONIZER PROCESSING CIRCUITS
BUFFERRED OUTPUTS TO C!
DOPPLER PROCESSING CIRCUITS
RG DATA
RG ALARMS
RG ALARMS, FAULTS
PHASE CODE CONTROL CIRCUITS
PHASE CODE
PERIODIC BITE CIRCUITS
TEST SIGNALS
INTERFACE CIRCUITS
TO TEST SET
TO/FROM ANTENNAS

Figure 2-1. Receiver Transmitter Functional Circuits.

2-2. TRANSMITTING CIRCUITS
(Figure 2-2)

Extremely stable and accurate RF frequencies are generated in the FMO. Frequency F0, the transmitting frequency, can have 21 different values as selected automatically by the microprocessor or manually by the test set. In either case, the frequency control is determined by the SFRQ( )H (STAMO Frequency High) signals received from the syncronizer microprocessor. The selected frequency F0 is phase modulated by the PHASE code signal and passed through a 30 dB coupler to the power amplifier AR1. The -30 dB output of coupler A17, F0, is available at jack J7 for monitoring and test purposes. Attenuator AT1 provides a 50-ohm termination for the coupler when the -30 dB output is not being used.

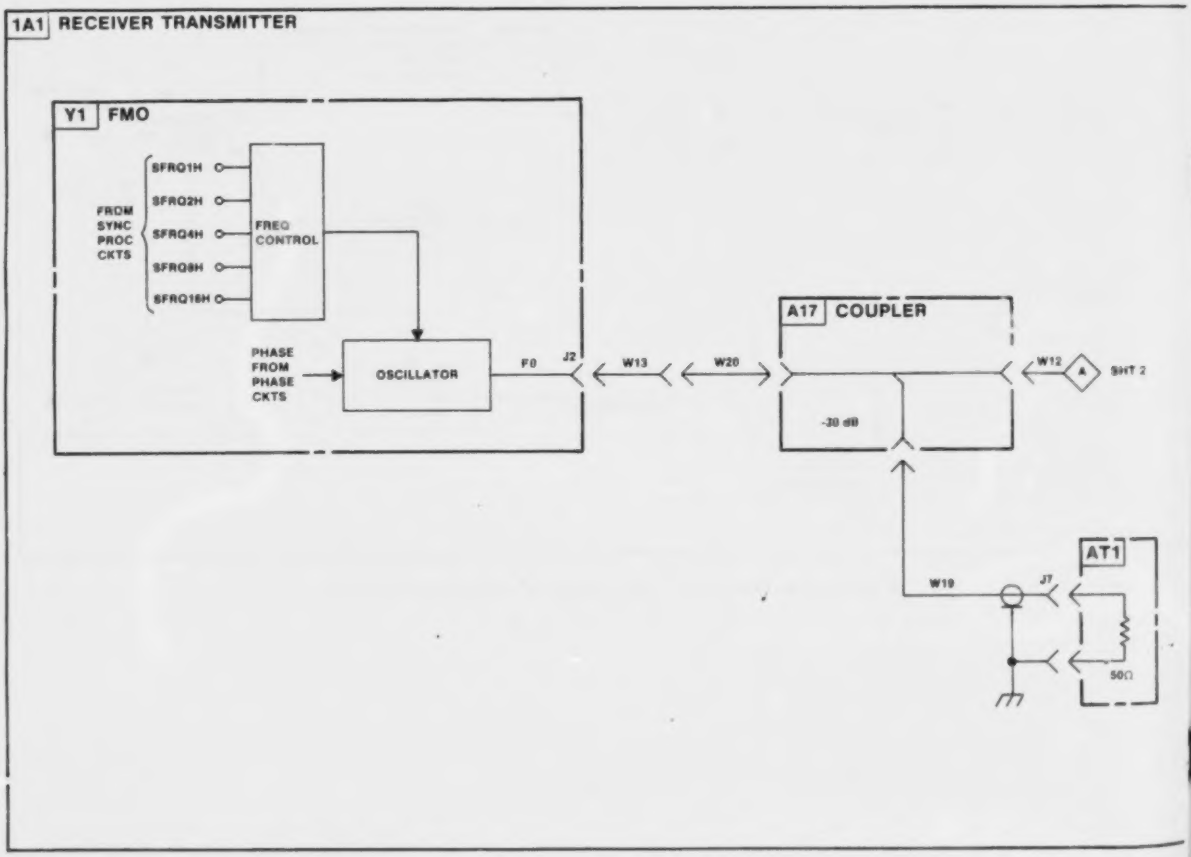

1A1 RECEIVER TRANSMITTER
Y1 FMO
FROM SYNC PROC CKTS
SFRQ1H
SFRQ2H
SFRQ4H
SFRQ8H
SFRQ16H
FREQ CONTROL
PHASE FROM PHASE CKTS
OSCILLATOR
F0
J2
W13
W20
A17 COUPLER
-30 dB
W12
A
SHT 2
W19
J7
AT1
50Ω

Figure 2-2. Transmitting Circuits (Sheet 1)

2-2. TRANSMITTING CIRCUITS (Continued)
(Figure 2-2)

In the power amplifier the F0 signal is modulated by the PRF (XMIT +, XMIT-) signals from the transmitter control circuits. After amplification to the level required for transmission, the power amplifier RF output signals (PARF) enter a circulator in the duplexer and are routed to the RF switch. The switch alternately connects the RF energy to the antennas via jacks J3, J4, J5, J6. The switching control signals (ANT 1, ANT 2) are produced in the antenna control circuits from system timing under control of the synchronizer microprocessor. In this configuration (V1), only two antennas are used, consequently, the duplexer output is switched between antenna jacks J3 and J4 only.

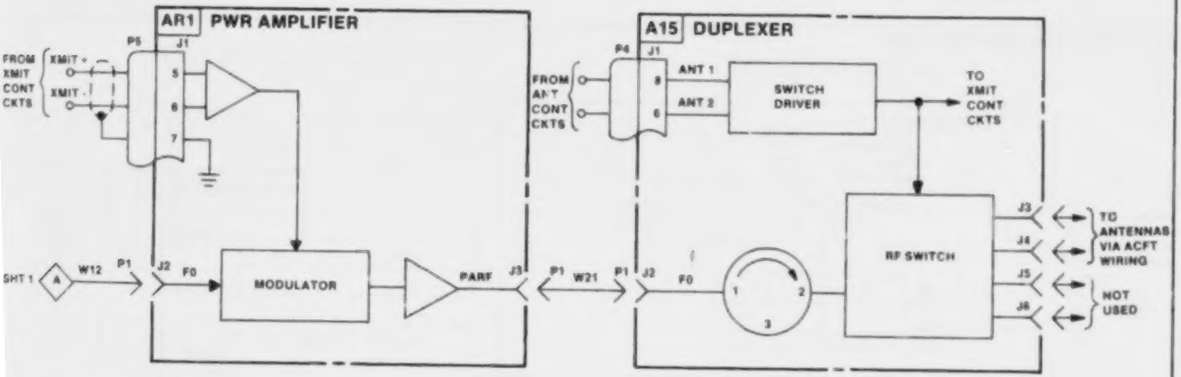

AR1 PWR AMPLIFIER
FROM XMIT CONT CKTS
XMIT +
XMIT -
P5
J1
5
6
7
SHT 1
A
W12
P1
J2
F0
MODULATOR
PARF
J3
P1
W21
P1
A15 DUPLEXER
FROM ANT CONT CKTS
P4
J1
8
6
ANT 1
ANT 2
SWITCH DRIVER
TO XMIT CONT CKTS
J2
F0
1
2
3
RF SWITCH
J3
J4
J5
J6
TO ANTENNAS VIA ACFT WIRING
NOT USED

Figure 2-2. Transmitting Circuits (Sheet 2)

2-3. RECEIVING CIRCUITS
(Figure 2-3)

The primary input signals to the receiving circuits are the radar return signals from the duplexer (RF SIG), and three RF signals from the FMO, (F1, F2, F3). In the receiving circuits, the RF signal passes through three IF mixer stages (triple conversion) where F1, F2, and F3 act as the local oscillator inputs. Frequency F1 MHz is used in the first conversion, and frequency F2, is used in the second conversion, both performed in the first IF assembly. Frequency F3, is used in the three final conversion stages performed in the second IF mixer/filter cards A2, A4, and A5. Three final conversion stages (all using F3 as a local oscillator signal) are required because the input is separated into three range-gated signals efore the final conversion. The F3 frequency is also used in the interference monitoring circuits and in the synchronizer (see synchronizer timing circuits) where it is used to derive all system timing. The power divider produces the four required F3 signals from the single F3 signal generated by the FMO.

Referring to figure 2-3, it can be seen that during the receive period, the radar return signals (RFSIG) from an antenna enter the duplexer and pass through the RF switch to the circulator. From port 3 of the circulator they pass to the first IF where these pulses are split into two separate channels, each being twice converted into a lower IF frequency. The first IF assembly outputs, IF INNER and IF OUTER, are then routed to the second IF card assemblies for range gating and final conversion to video (a series of pulses containing doppler information - if a target was present).

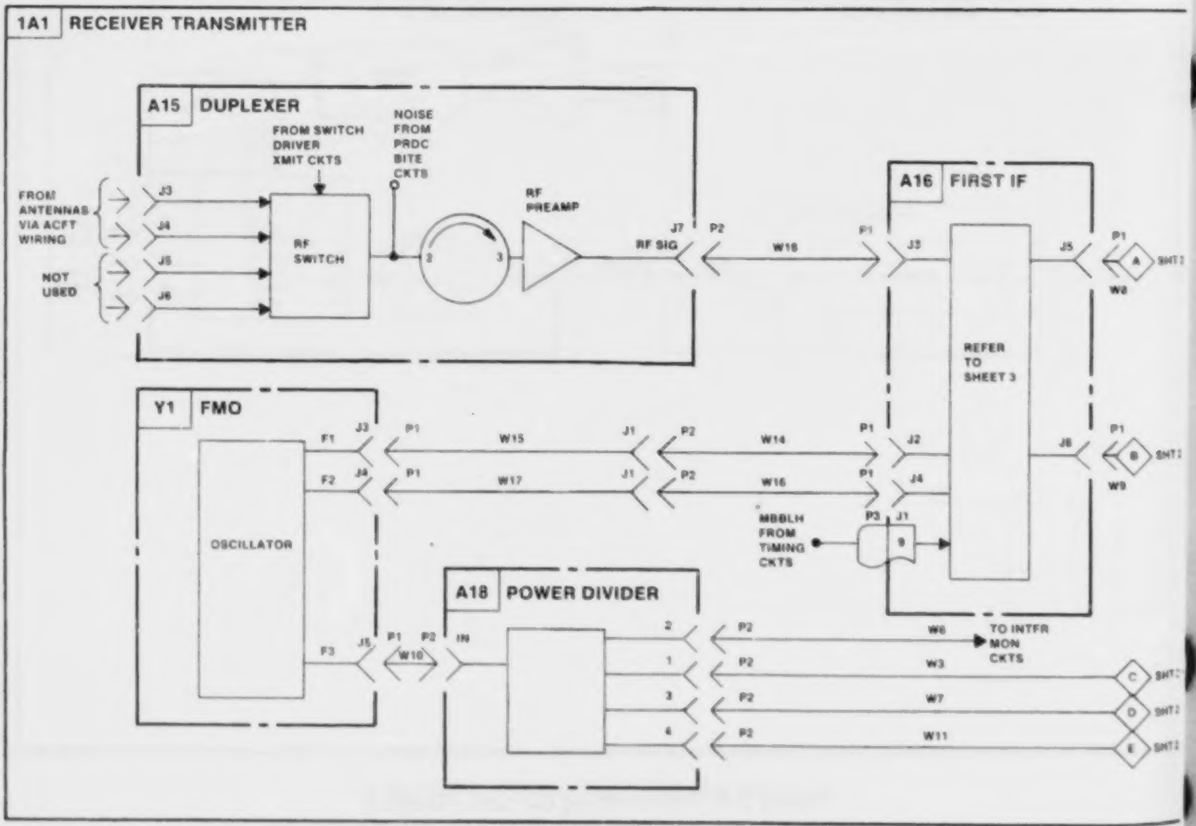

1A1 RECEIVER TRANSMITTER
A15 DUPLEXER
FROM SWITCH DRIVER XMIT CKTS
NOISE FROM PRDC BITE CKTS
FROM ANTENNAS VIA ACFT WIRING
NOT USED
J3
J4
J5
J6
RF SWITCH
2
3
RF PREAMP
J7
RF SIG
P2
W18
P1
A16 FIRST IF
J3
REFER TO SHEET 3
J5
P1
A
SHT
W8
Y1 FMO
OSCILLATOR
F1
J3
P1
W15
J1
P2
W14
P1
J2
F2
J4
P1
W17
J1
P2
W16
P1
J4
J8
P1
B
SHT
W9
MBBLH FROM TIMING CKTS
P3
J1
9
A18 POWER DIVIDER
F3
J5
P1
P2
W10
IN
2
1
3
4
P2
W6
TO INTFR MON CKTS
W3
C
SHT
W7
D
SHT
W11
E
SHT

Figure 2-3. Receiving Circuits (Sheet 1)

2-3. RECEIVING CIRCUITS (Continued)
(Figure 2-3)

The IF INNER signal goes to the A1 card in the second IF where it is gated with R1+, R1-, to produce the RG1 signal. This is then mixed in card A2 with F3 to produce RG1 (range gate 1) DATA, the range gate 1 video signal. The IF OUTER signal is divided into three parts in the A3 card, one part being range gated with R2+, R2-, to produce an RG2 signal and another with R3+, R3-, to produce a RG3 signal. The third part is used in the interference monitoring circuits. The RG2 signal is then mixed with F3 in the A4 card to produce RG2 DATA, while the RG3 signal goes to the A5 card where it is mixed with F3 to produce the RG3 DATA. The three video signals (RG1 DATA, RG2 DATA, and RG3 DATA) are sent to the doppler processing circuits for further processing and conversion to range gate alarms if they contain significant doppler information.

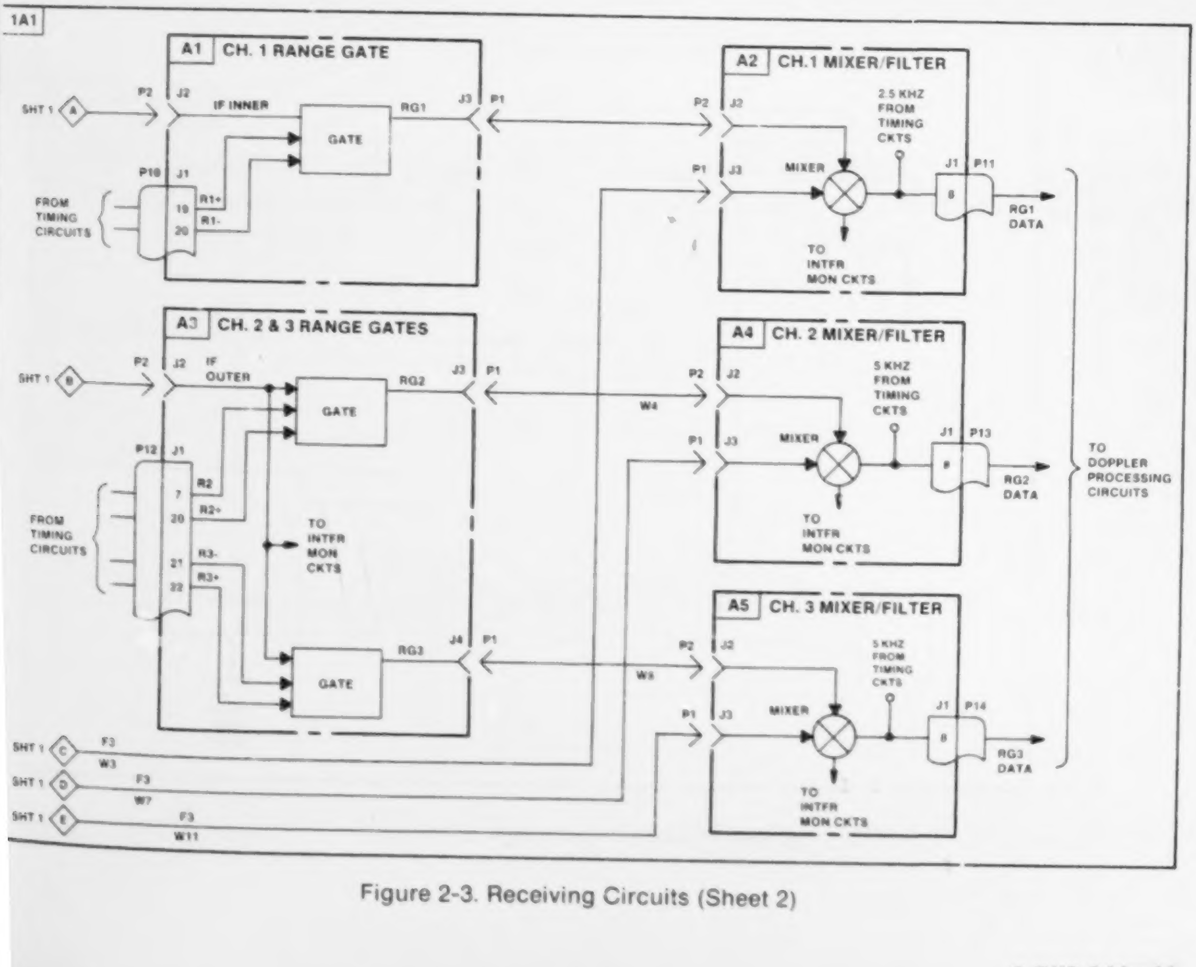

1A1
A1 CH. 1 RANGE GATE
SHT 1 A
P2
J2
IF INNER
GATE
RG1
J3
P1
P10
J1
FROM TIMING CIRCUITS
19
20
R1+
R1-
A3 CH. 2 & 3 RANGE GATES
SHT 1 B
P2
J2
IF OUTER
GATE
RG2
J3
P1
P12
J1
FROM TIMING CIRCUITS
7
20
21
22
R2
R2+
R3-
R3+
TO INTFR MON CKTS
GATE
RG3
J4
P1
SHT 1 C
F3
W3
SHT 1 D
F3
W7
SHT 1 E
F3
W11
A2 CH.1 MIXER/FILTER
P2
J2
2.5 KHZ FROM TIMING CKTS
P1
J3
MIXER
J1
P11
8
RG1 DATA
TO INTFR MON CKTS
A4 CH. 2 MIXER/FILTER
P2
J2
W4
5 KHZ FROM TIMING CKTS
P1
J3
MIXER
J1
P13
8
RG2 DATA
TO INTFR MON CKTS
A5 CH. 3 MIXER/FILTER
P2
J2
W8
5 KHZ FROM TIMING CKTS
P1
J3
MIXER
J1
P14
8
RG3 DATA
TO INTFR MON CKTS
TO DOPPLER PROCESSING CIRCUITS

Figure 2-3. Receiving Circuits (Sheet 2)

2-3. RECEIVING CIRCUITS (Continued)
(Figure 2-3)

We noted that the first IF assembly converted the input signal into two channels and each went through two frequency conversions. Figure 2-3, sheet 3 shows some additional functions which occur within this assembly. It can be seen that the input signal (RF SIG) and two mixer signals (F1 and F2) are all applied to couplers to produce the two channel outputs. Also, a third coupler sends a part of RF SIG and MBBLH signal to the interference monitoring circuits. The MBBLH (main bang blank high) signal which occurs during transmit time, is applied to gates in the first IF. It effectively opens the IF INNER and OUTER lines during the transmitting period to prevent noise signals from entering the second IF card assemblies. (Main bang is a radar term meaning the transmitted pulse.)

In summary, the receiving circuits convert the RF input (RF SIG) into three range-gated video signals (RG1 DATA, RG2 DATA, RG3 DATA) which are inputs to the doppler processing circuits. The 2.5 and 5 kHz signals shown on the A2, A4 and A5 cards are simulated outputs of the receiving circuits which occur during periodic BITE (Built In Test Equipment) test. Also, a noise signal is produced in the duplexer during BITE test (see periodic BITE circuits).

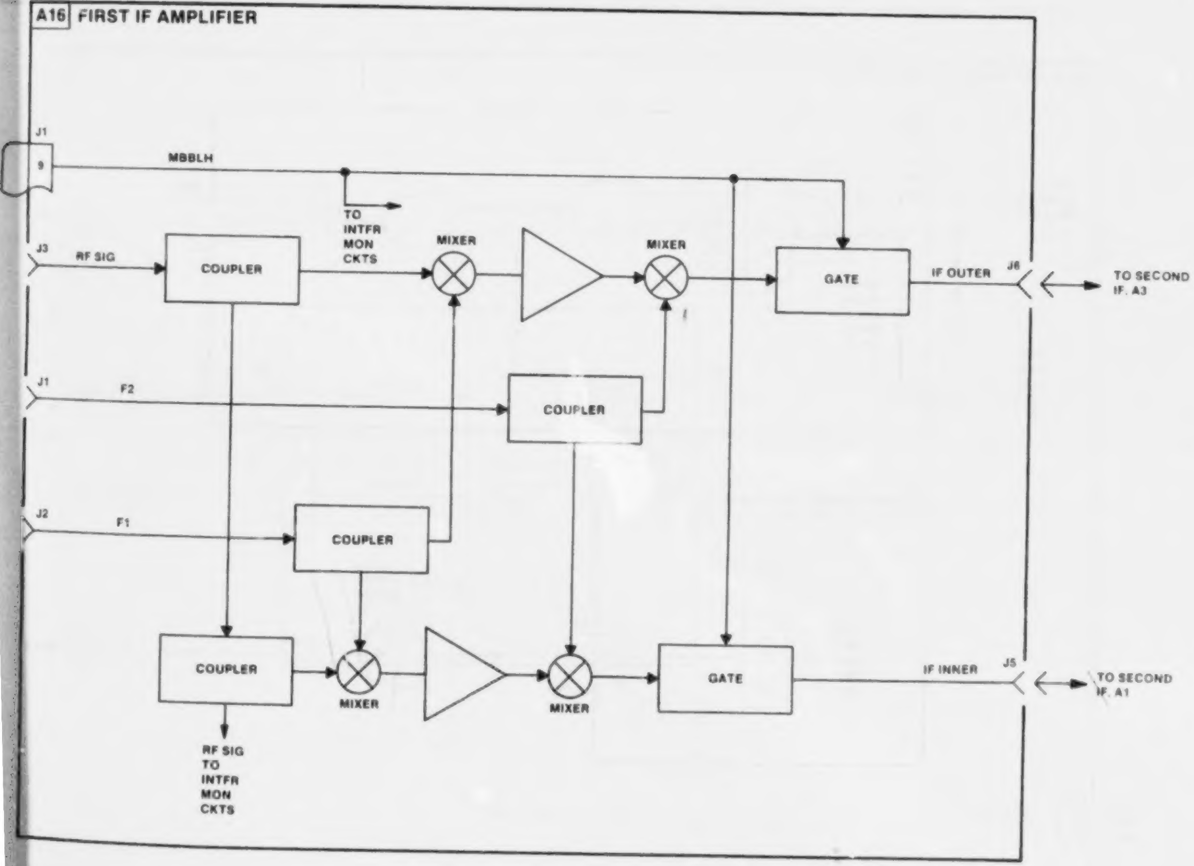

A16
FIRST IF AMPLIFIER
J1
9
MBBLH
TO
INTFR
MON
CKTS
J3
RF SIG
COUPLER
MIXER
MIXER
GATE
IF OUTER
J6
TO SECOND
IF. A3
J1
F2
COUPLER
J2
F1
COUPLER
COUPLER
MIXER
MIXER
GATE
IF INNER
J5
TO SECOND
IF. A1
RF SIG
TO
INTFR
MON
CKTS

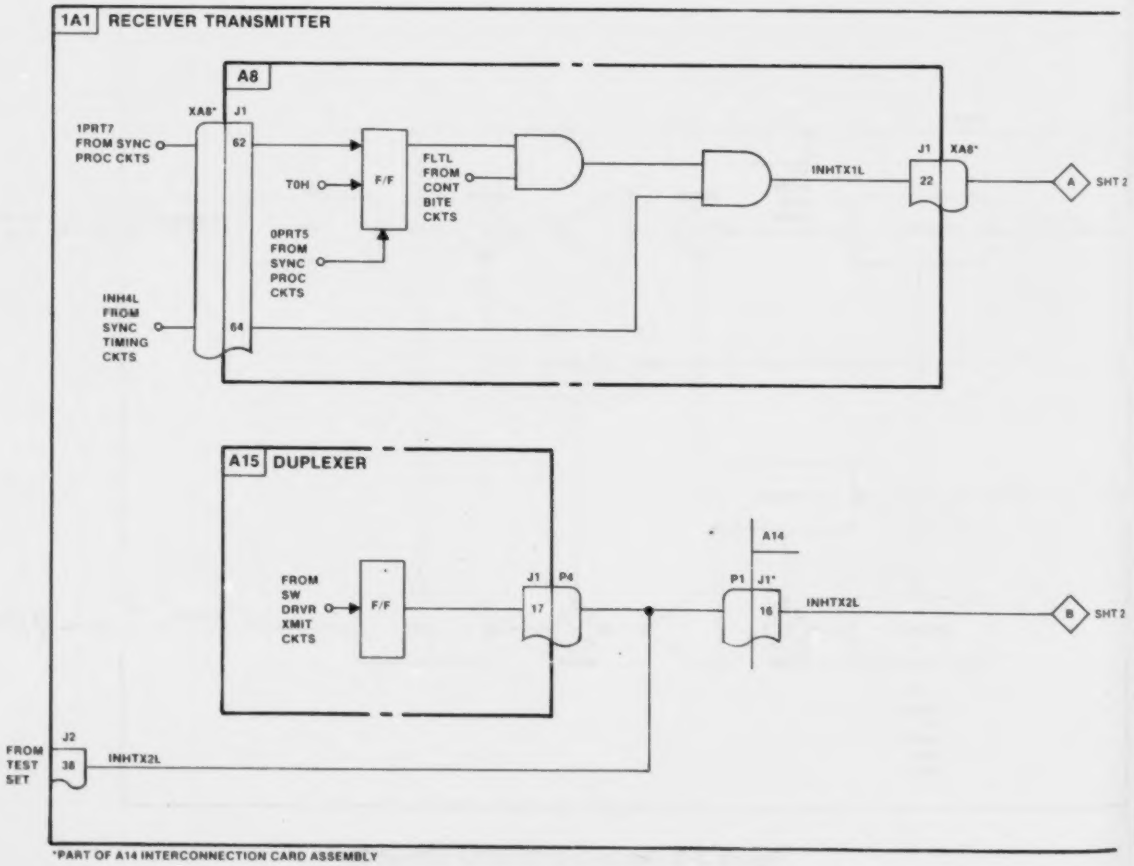
Figure 2-3. Receiving Circuits (Sheet 3)

2-4. TRANSMITTER CONTROL CIRCUITS
(Figure 2-4)

We have seen how the transmitting circuits require the modulating signal (XMIT+, XMIT-) to produce the modulated RF signal radiated by the antennas. If the modulating signal is not present, no modulation will occur, and the transmitting circuits (specifically, the power amplifier) are disabled. This disabling of the transmitter, which is desirable and required under certain conditions of operation, is accomplished by the transmitter control circuits. Referring to figure 2-4, it can be seen that the XMIT+, XMIT- signals are derived in the A7 card. These signals are produced from the XMIT signal produced by the timing circuits. However, the output will be present (gated out) only if the two INHTX( )L signals are not present.

The INHTX2L (Inhibit Transmitter 2 Low) signal is derived from a timed delay triggered by the switch driver in the transmitting circuits. This signal occurs each time the duplexer RF switch moves from one position to the other. During this brief interval the RF power from the power amplifier is unloaded as it is not connected to either antenna. Consequently, it is desirable that the transmitting circuits are disabled under this condition.

During bench test using the test set, the INHTX2L signal is generated by placing the test set XMTR switch in the DISABLE position. This allows testing of the RT without transmitter operation.


1A1
RECEIVER TRANSMITTER
A8
XA8*
J1
1PRT7
FROM SYNC
PROC CKTS
62
TOH
F/F
FLTL
FROM
CONT
BITE
CKTS
0PRTS
FROM
SYNC
PROC
CKTS
INHTX1L
J1
XA8*
22
A
SHT 2
INH4L
FROM
SYNC
TIMING
CKTS
64
A15
DUPLEXER
FROM
SW
DRVR
XMIT
CKTS
F/F
J1
P4
17
A14
P1
J1*
16
INHTX2L
B
SHT 2
FROM
TEST
SET
J2
38
INHTX2L

*PART OF A14 INTERCONNECTION CARD ASSEMBLY

Figure 2-4. Transmitter Control Circuits (Sheet 1)

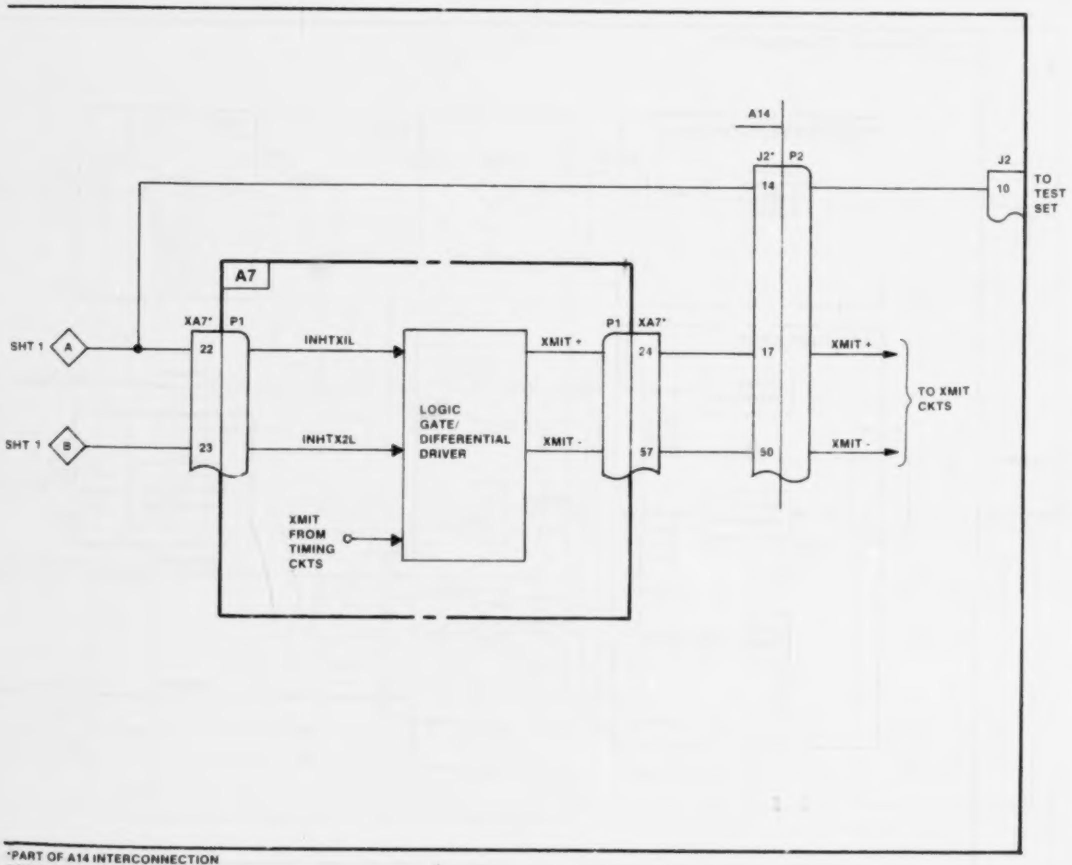
2-4. TRANSMITTER CONTROL CIRCUITS (Continued) (Figure 2-4)

The INHTX1L signal performs the same role in disabling the transmitter but for different reasons. This signal is generated in the A8 card under several conditions of operation. It will occur if the INH4L, FLTL or 1PRT7 signals are present.

The FLTL (Fault Low) signal from the continuous BITE circuits will enable the INHTX1L signal. As will be shown, this signal occurs if any of the continuous BITE or periodic BITE checks fail. Failure of BITE indicates system malfunction, so obviously it is desirable to shut-down transmitter operation under this condition.

A low logic level on the microprocessor output 1PRT7 is a second way in which the INHTX1L signal is enabled. In this case, the transmitter is inhibited by microprocessor command. This is initiated under several conditions of operation as controlled by the program stored in the PROM (programmable read only memory).

Refer to the classified supplement, TM 11-5865-201-30-2, for a discussion of the INH4L input.


A14
J2*
P2
14
J2
10
TO TEST SET
A7
XA7*
P1
SHT 1
A
22
INHTXIL
SHT 1
B
23
INHTX2L
LOGIC GATE/ DIFFERENTIAL DRIVER
XMIT FROM TIMING CKTS
XMIT +
XMIT -
P1
XA7*
24
57
17
50
XMIT +
XMIT -
TO XMIT CKTS

*PART OF A14 INTERCONNECTION CARD ASSEMBLY

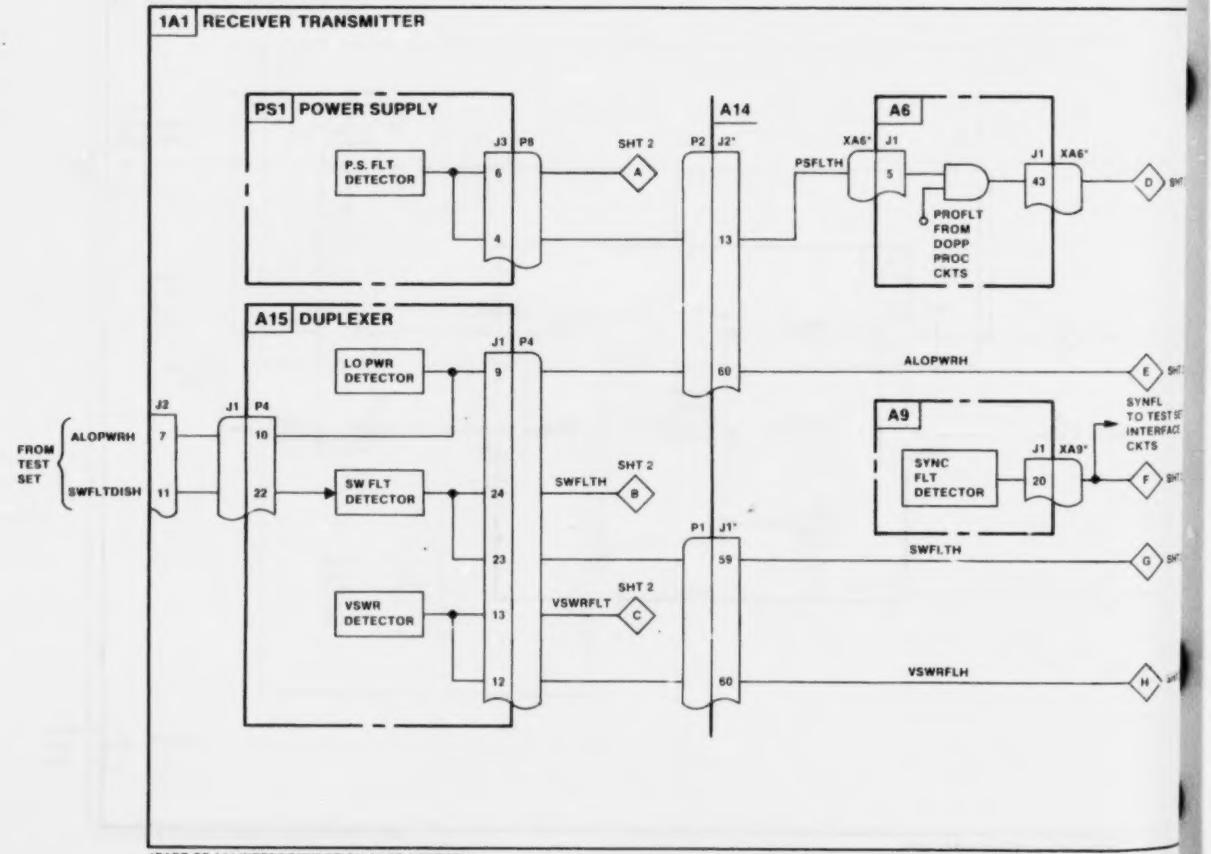
Figure 2-4. Transmitter Control Circuits (Sheet 2)

2-5. CONTINUOUS BITE CIRCUITS
(Figure 2-5)

The countermeasures set is provided with BITE (built-in-test equipment) to monitor system performance, and to shut it down in the event of system malfunction or degraded performance. Two types of BITE are used; continuous BITE and periodic BITE. The continuous BITE monitors the following system parameters:

- Transmitter power output
- Antenna VSWR (Voltage Standing Wave Ratio)
- Duplexer switch operation
- Synchronizer operation
- Doppler processor operation
- Power supply operation
- Power amplifier temperature

The power supply contains a fault detector which outputs a power supply fault high (PSFLTH) signal in the event of a power supply failure. A processor fault (PROFLT) will be produced by the doppler processor if its internal processor BITE circuits detect a processor failure. These signals are gated in the A6 card and are sent to an AND gate in the A8 card as a PROC PSFLTH signal. The AND gate also has fault inputs from three fault detectors in the duplexer. These will occur under an antenna low power condition (ALOPWRH), duplexer switch failure (SWFLTH), or a high VSWR fault condition (VSWRFLH).


1A1 RECEIVER TRANSMITTER
PS1 POWER SUPPLY
P.S. FLT DETECTOR
J3
P8
6
4
SHT 2
A
A14
P2
J2*
13
PSFLTH
A6
XA6*
J1
5
PROFLT FROM DOPP PROC CKTS
J1
XA6*
43
D
A15 DUPLEXER
J1
P4
LO PWR DETECTOR
9
60
ALOPWRH
E
FROM TEST SET
ALOPWRH
SWFLTDISH
J2
7
11
J1
P4
10
22
SW FLT DETECTOR
24
23
SWFLTH
SHT 2
B
A9
SYNC FLT DETECTOR
J1
XA9*
20
SYNFL TO TEST SET INTERFACE CKTS
F
P1
J1*
59
SWFLTH
G
VSWR DETECTOR
13
12
VSWRFLT
SHT 2
C
60
VSWRFLH
H

*PART OF A14 INTERCONNECTION CARD ASSEMBLY

Figure 2-5. Continuous BITE Circuits (Sheet 1)

2-5. CONTINUOUS BITE CIRCUITS (Continued) (Figure 2-5)

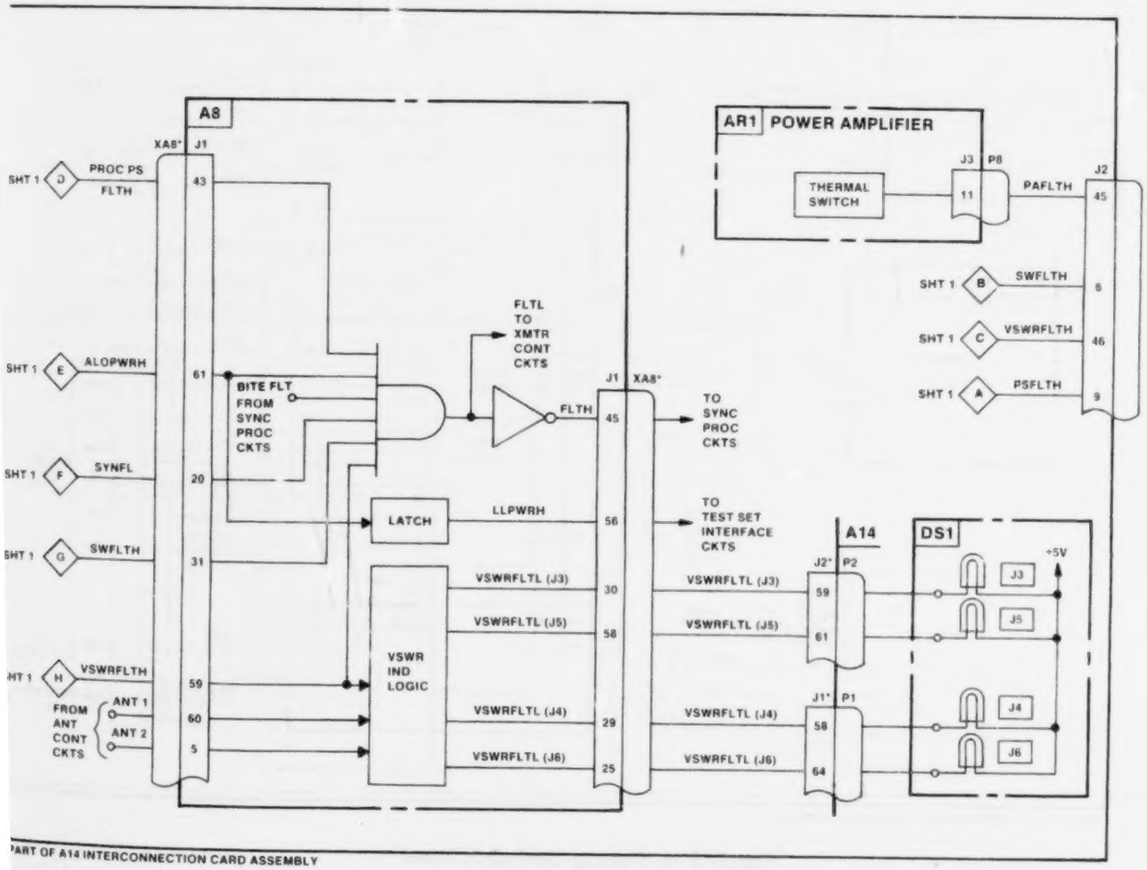
Two other fault inputs to the AND gate are SYNFL which occurs if the synchronizer fails, and a BITEFLT which would occur if the periodic BITE check is failed. All of these fault signals are gated together so that whenever any one occurs, a FLTL (and FLTH) signal is produced. The FLTL signal is routed to the transmitter control circuits to stop transmitter operation while the FLTH signal is applied to the synchronizer processor circuits to produce an INOP indication.

The VSWRFLH signal is also applied to logic circuits on the A8 card along with antenna position information (ANT 1, ANT 2) to produce one of four VSWRFLT signals (one of two for the V1 configuration). This will light the appropriate lamp (J3, J4, J5, J6) on the RT indicator DS1.

The low power signal is latched in the A8 card (LLPWPH) and routed to the test set to light the BITE FAULT LOW PWR indicator. The other fault signals are also applied directly to the test set to light corresponding BITE FAULT indicators.

The PROFLT signal generated in the A6 card (refer to doppler processing circuits) and the SYNFL signal pass through buffer stages on the A6 card before being sent to the test set to light corresponding BITE FAULT indicators.

The power amplifier contains a thermal switch which is actuated if the amplifier overheats and shuts it down. This condition (no power) will cause the low power detector to be activated. Note that both the low power and switch fault detectors may be disabled by the ALOPWRH (antenna low power high) and SWFLTDISH (switch fault disable high) test signals from the test set.


A8
XA8*
J1
SHT 1
D
PROC PS FLTH
43
SHT 1
E
ALOPWRH
61
BITE FLT FROM SYNC PROC CKTS
SHT 1
F
SYNFL
20
SHT 1
G
SWFLTH
31
SHT 1
H
VSWRFLTH
59
FROM ANT CONT CKTS
ANT 1
ANT 2
60
5
FLTL TO XMTR CONT CKTS
FLTH
J1
XA8*
45
TO SYNC PROC CKTS
LATCH
LLPWRH
56
TO TEST SET INTERFACE CKTS
VSWR IND LOGIC
VSWRFLTL (J3)
30
VSWRFLTL (J5)
58
VSWRFLTL (J4)
29
VSWRFLTL (J6)
25
AR1
POWER AMPLIFIER
THERMAL SWITCH
J3
P8
11
PAFLTH
J2
45
SHT 1
B
SWFLTH
6
SHT 1
C
VSWRFLTH
46
SHT 1
A
PSFLTH
9
TO TEST SET
A14
J2*
P2
VSWRFLTL (J3)
59
VSWRFLTL (J5)
61
J1*
P1
VSWRFLTL (J4)
58
VSWRFLTL (J6)
64
DS1
+5V
J3
J5
J4
J6

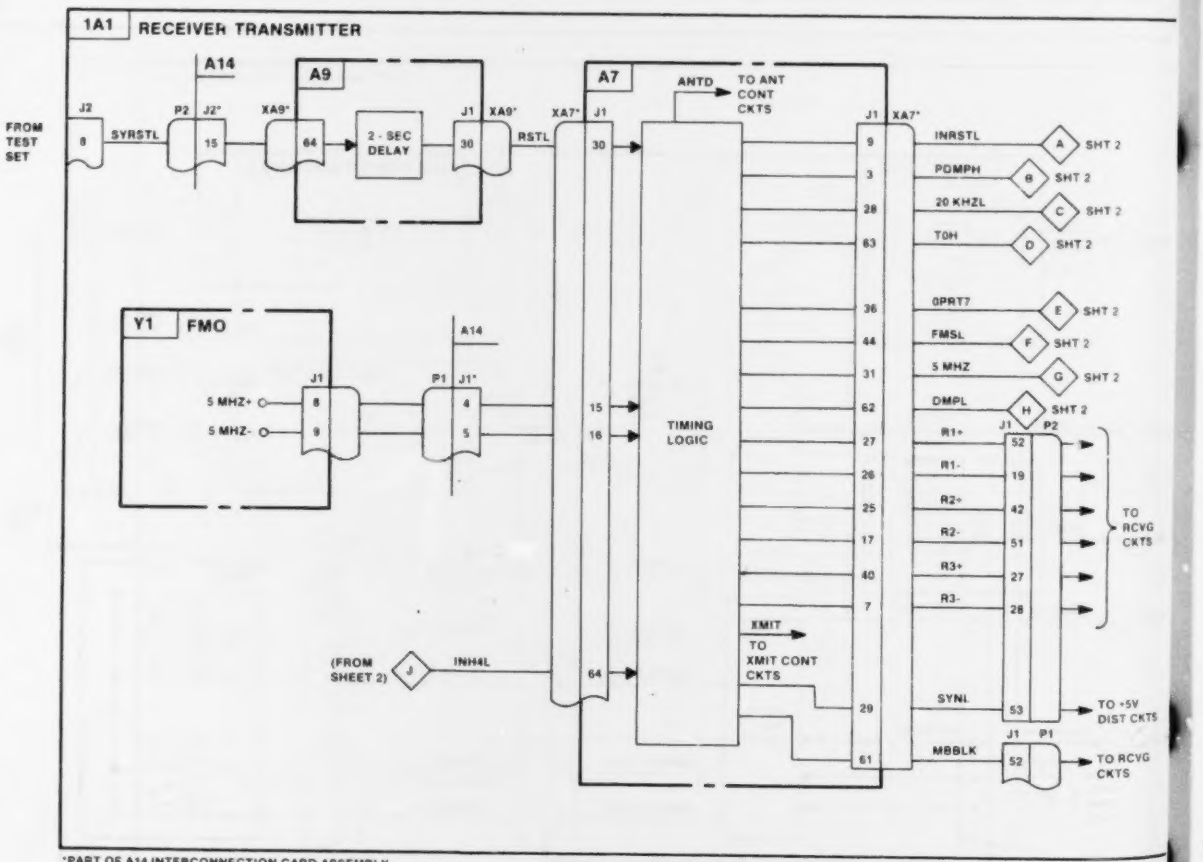
ART OF A14 INTERCONNECTION CARD ASSEMBLY

Figure 2-5. Continuous BITE Circuits (Sheet 2)

2-6. TIMING CIRCUITS
(Figure 2-6)

The timing circuits produce all the timing signals required for operation of the countermeasures set. Most of the timing signals are generated in the A7 card assembly of the synchronizer. The differential output signals 5 MHz+/5 MHz- from the FMO, which are derived in its stable oscillator, are routed to the A7 card and are used to produce all lower frequency timing signals by means of counters, dividers, and PROMs (Programmable Read Only Memory) comprising the timing logic. A timing diagram showing the relationships between the major timing circuits outputs is provided in the classified supplement to this manual.

As you can see from the functional diagram, the timing logic outputs are used within the A7 card assembly itself and are routed to the A6, A8, A9, A13, A1 and A3 card assemblies. The A8 card contains a divider to provide the 5 kHz and 2.5 kHz signals from the 20 kHz input. Also, timing logic within the A6 card produces additional timing signal outputs (MIENL, INH4L) from timing signal inputs from the A7 card assembly. A pulse stretcher within the second IF A1 card assembly provides ECMR pulses to the interference monitoring circuits.


1A1
RECEIVER TRANSMITTER
FROM TEST SET
J2
8
SYRSTL
A14
P2
J2*
15
A9
XA9*
64
2 - SEC DELAY
J1
30
XA9*
RSTL
A7
XA7*
J1
30
ANTD
TO ANT CONT CKTS
Y1
FMO
5 MHZ+
5 MHZ-
J1
8
9
A14
P1
J1*
4
5
15
16
TIMING LOGIC
(FROM SHEET 2)
J
INH4L
64
XMIT
TO XMIT CONT CKTS
J1
XA7*
9
3
28
63
36
44
31
62
27
26
25
17
40
7
29
61
INRSTL
A
SHT 2
PDMPH
B
SHT 2
20 KHZL
C
SHT 2
TOH
D
SHT 2
0PRT7
E
SHT 2
FMSL
F
SHT 2
5 MHZ
G
SHT 2
DMPL
H
SHT 2
J1
P2
R1+
52
R1-
19
R2+
42
R2-
51
R3+
27
R3-
28
TO RCVG CKTS
SYNL
53
TO +5V DIST CKTS
J1
P1
MBBLK
52
TO RCVG CKTS

*PART OF A14 INTERCONNECTION CARD ASSEMBLY

Figure 2-6. Timing Circuits (Sheet 1)

2-6. TIMING CIRCUITS (Continued)
(Figure 2-6)

The timing circuits can be reset by the SYRSTL (system reset low) from the test set; this occurs when the test set PROGRAM switch is set to RESET. The SYRSTL enables a pulse stretcher to produce a RSTL (reset low) pulse which resets the microprocessor in the synchronizer processor circuits as well as the timing circuits.

The purpose of the individual timing signals are explained in functional circuits where they are used.

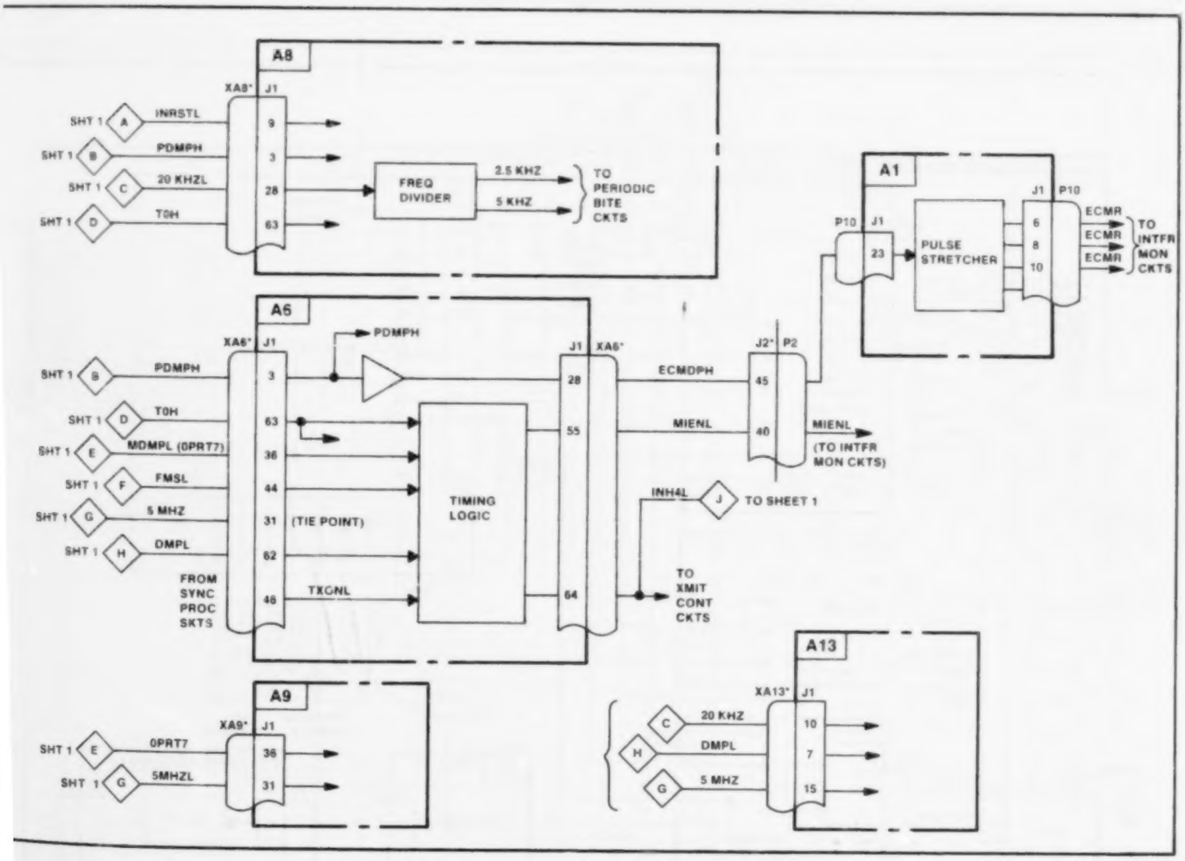

A8
XA8*
J1
SHT 1
A
INRSTL
9
SHT 1
B
PDMPH
3
SHT 1
C
20 KHZL
28
SHT 1
D
T0H
63
FREQ DIVIDER
2.5 KHZ
5 KHZ
TO PERIODIC BITE CKTS
A6
XA6*
J1
PDMPH
SHT 1
B
PDMPH
3
SHT 1
D
T0H
63
SHT 1
E
MDMPL (0PRT7)
36
SHT 1
F
FMSL
44
SHT 1
G
5 MHZ
31
(TIE POINT)
SHT 1
H
DMPL
62
FROM SYNC PROC SKTS
TXGNL
46
TIMING LOGIC
J1
XA6*
28
55
64
ECMDPH
MIENL
INH4L
J
TO SHEET 1
TO XMIT CONT CKTS
J2*
P2
45
40
MIENL
(TO INTFR MON CKTS)
A1
P10
J1
23
PULSE STRETCHER
J1
P10
6
8
10
ECMR
ECMR
ECMR
TO INTFR MON CKTS
A9
XA9*
J1
SHT 1
E
0PRT7
36
SHT 1
G
5MHZL
31
A13
XA13*
J1
C
20 KHZ
10
H
DMPL
7
G
5 MHZ
15

Figure 2-6. Timing Circuits (Sheet 2)

2-7. SYNCHRONIZER PROCESSOR CIRCUITS (Figure 2-7)

The synchronizer processor circuits receive range gate alarms, interference signals, control signals and timing signals. From these inputs the microprocessor, under control of system program stored in the PROM (Programmable Read Only Memory), produces output commands which control system operation.

The microprocessor used has two 8-line ports. Port zero (0PRT) is used for input data only while port one (1PRT) is used for both input and output data at different times during the signal processing interval.

The port zero inputs enter the microprocessor from the A7, A6, and A8 card assemblies. The range gate alarms (RG1, 2, 3 ALARMS), large signal (LSDLL) and mutual interference (MIC1L) inputs, two of the three ECM signals, and the test two control signal (TST2L) are applied to a multiplexer on the A7 card. The ECM3 and TST1L signals are applied to a mutliplexer on the A6 card. The multiplexers alternately connect one signal of each pair to a port zero input line. For example, the RG1 ALARML and the ECMIL inputs are alternately connected to port zero line 1 (0PRT1), and the timing is such that the microprocessor knows which of these two signals it is receiving. As you can see, the input signals mentioned enter the microprocessor on the 0PRT0 , 0PRT1, 0PRT2, 0PRT3 and 0PRT6 lines. The WRMUPL (Warmup) signal enters on 0PRT4 while 0PRT5 receives a gated signal related to the "standby" mode (see control indicator control circuits) and system warmup. The 0PRT7 line receives a timing signal from the timing circuits on the A7 card.

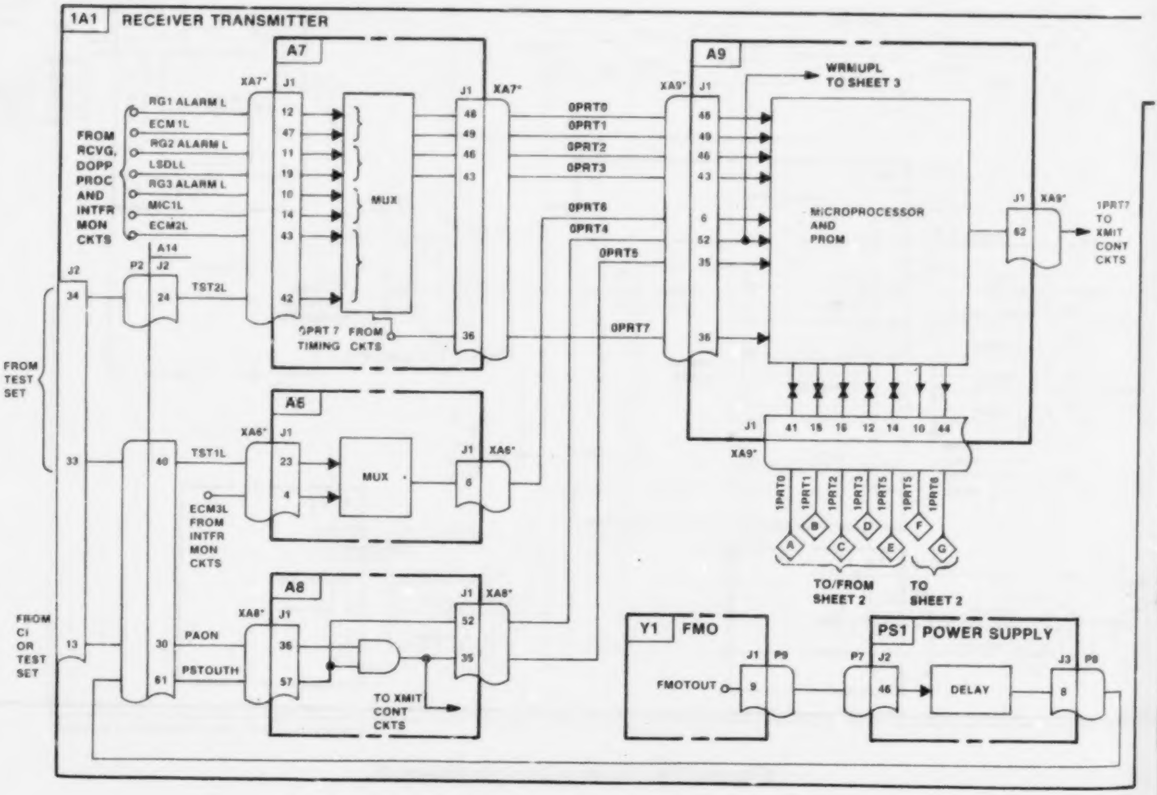

1A1
RECEIVER TRANSMITTER
A7
XA7*
J1
RG1 ALARM L
ECM1L
RG2 ALARM L
LSDLL
RG3 ALARM L
MIC1L
ECM2L
FROM RCVG, DOPP PROC AND INTFR MON CKTS
12
47
11
19
10
14
43
42
MUX
48
49
46
43
36
0PRT 7 FROM TIMING CKTS
A14
J2
P2
34
24
TST2L
FROM TEST SET
33
40
TST1L
A6
XA6*
23
4
ECM3L FROM INTFR MON CKTS
6
A8
XA8*
FROM CI OR TEST SET
13
30
PAON
61
PSTOUTH
36
57
52
35
TO XMIT CONT CKTS
0PRT0
0PRT1
0PRT2
0PRT3
0PRT6
0PRT4
0PRT5
0PRT7
A9
XA9*
WRMUPL TO SHEET 3
MICROPROCESSOR AND PROM
6
52
35
62
1PRT7 TO XMIT CONT CKTS
41
15
16
12
14
10
44
1PRT0
1PRT1
1PRT2
1PRT3
1PRT5
1PRT5
1PRT6
A
B
C
D
E
F
G
TO/FROM SHEET 2
TO SHEET 2
Y1
FMO
FMOTOUT
J1
P9
9
PS1
POWER SUPPLY
P7
J2
46
DELAY
J3
P8
8

Figure 2-7. Synchronizer Processor Circuits (Sheet 1)

2-7. SYNCHRONIZER PROCESSOR CIRCUITS (Continued) (Figure 2-7)

The remaining input signals enter the microprocessor on five of its port one lines (see sheet 2). The five binary frequency FRQS ( ) L signals are from the test set and determine what FMO transmitting channel will be used. These signals enter the microprocessor on its 1PRT0 through 1PRT4 lines. Gates enabled by a delayed pulse from the 1PRT6 control signal during system reset (SYRSTH) allow the FRQS( )L signals to be inputted into the microprocessor without affecting the storage registers.

Now let us look at the microprocessor outputs from port one. The 1PRT0 through 1PRT5 outputs are applied to storage registers A and B.

The 1PRT0 line has two outputs, SFRQIH (Stamo Frequency - Stamo is a synonym for FMO) and BITEH at different times. When the SFRQIH signal is outputted, the 1PRT6 line enables storage register A applying this signal to the FMO and to the test set. Similarly, when the BITEH signal is outputted, the 0PRT6 line enables storage register B applying this signal to the periodic BITE circuits. You can see that all the SFRQ( )H signals go to the FMO, where they will select the transmit channel, and also to the test set where they control the RT CHANNEL indicator readout. The one remaining output of storage register A is the TXONL (transmitter on) command which controls mutual interference detection (see interference monitoring circuits).

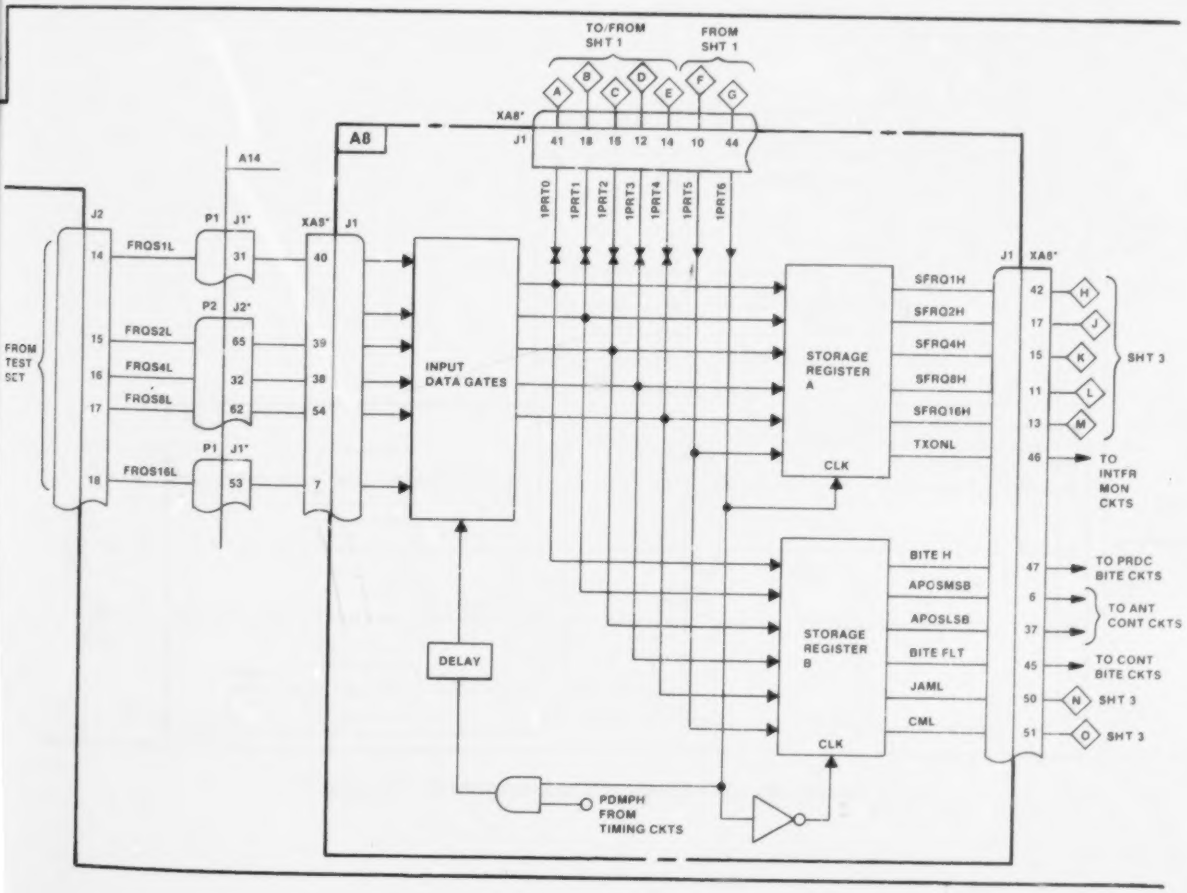

TO/FROM SHT 1
FROM SHT 1
A
B
C
D
E
F
G
XA8*
J1
41
18
16
12
14
10
44
A8
1PRT0
1PRT1
1PRT2
1PRT3
1PRT4
1PRT5
1PRT6
A14
J2
P1
J1*
XA8*
J1
FRQS1L
14
31
40
P2
J2*
FRQS2L
15
65
39
FRQS4L
16
32
38
FRQS8L
17
62
54
P1
J1*
FRQS16L
18
53
7
FROM TEST SET
INPUT DATA GATES
STORAGE REGISTER A
CLK
SFRQ1H
SFRQ2H
SFRQ4H
SFRQ8H
SFRQ16H
TXONL
J1
XA8*
42
17
15
11
13
46
H
J
K
L
M
SHT 3
TO INTFR MON CKTS
STORAGE REGISTER B
CLK
BITE H
APOSMSB
APOSLSB
BITE FLT
JAML
CML
47
6
37
45
50
51
TO PRDC BITE CKTS
TO ANT CONT CKTS
TO CONT BITE CKTS
N
SHT 3
O
SHT 3
DELAY
PDMPH FROM TIMING CKTS

Figure 2-7. Synchronizer Processor Circuits (Sheet 2)

2-7. SYNCHRONIZER PROCESSOR CIRCUITS (Continued) (Figure 2-7)

The storage register B outputs are also microprocessor commands from port 1, lines 0 to 5. The BITEH command enables the periodic BITE check. The APOMSB and APOLSB (Antenna Position Most/Least Significant BIT) control antenna selection (see antenna control circuits). The BITE FAULT output occurs as a result of periodic BITE check failure, and is AND'ed with other possible faults in the continuous BITE circuits. (The output of these circuits is the FLTH signal which is applied to the isolator stage on the A9 card here in the synchronizer processor circuits.) The JAML, CML, and WRMUPL signals also are applied to isolator stages on the A9 card before being sent to the control indicator or test set.

Line 7 of port one (sheet 1) is the only output which is not applied to the storage registers. It is routed to the transmitter control circuits where it inhibits the transmitter under certain conditions of operation.

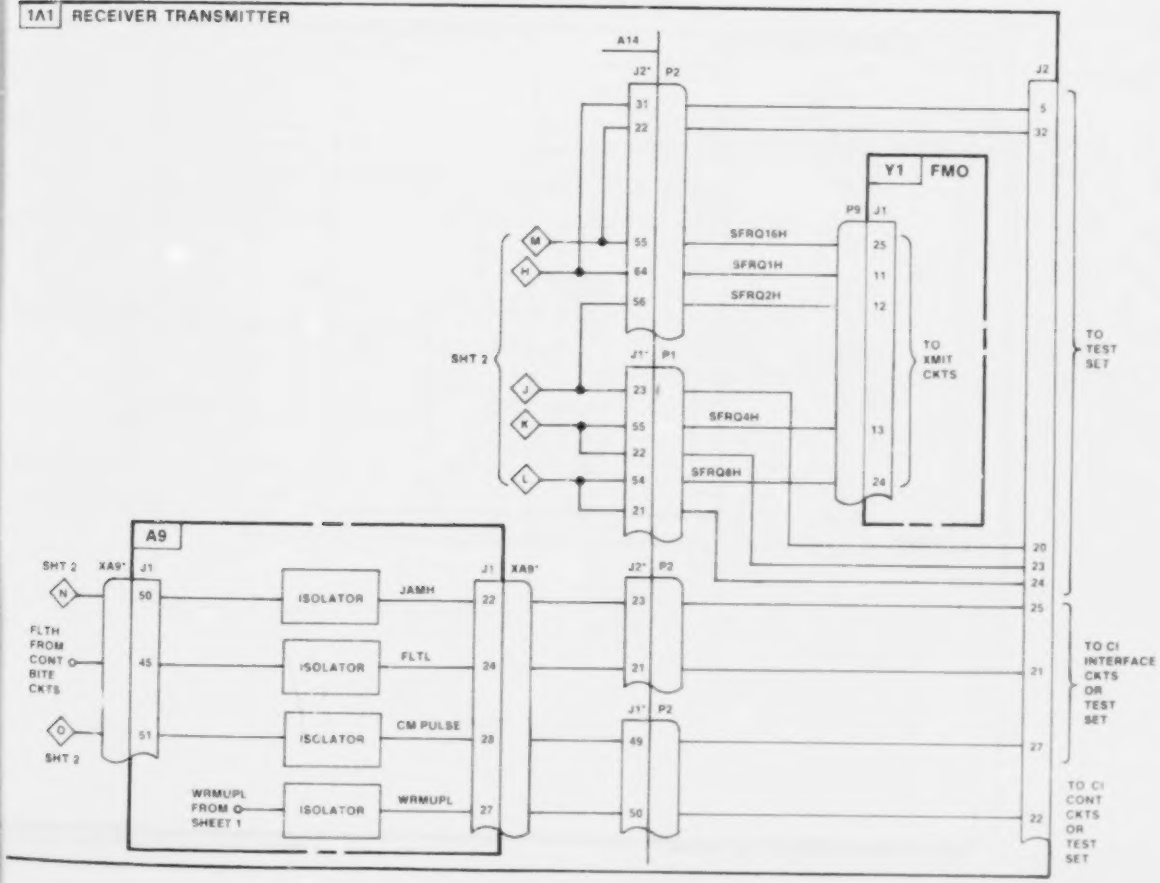

1A1 RECEIVER TRANSMITTER
A14
J2* P2
31
22
55
64
56
J1* P1
23
55
22
54
21
M
H
J
K
L
SHT 2
Y1 FMO
P9 J1
SFRQ16H
SFRQ1H
SFRQ2H
SFRQ4H
SFRQ8H
25
11
12
13
24
TO XMIT CKTS
J2
5
32
20
23
24
25
21
27
22
TO TEST SET
TO CI INTERFACE CKTS OR TEST SET
TO CI CONT CKTS OR TEST SET
A9
SHT 2
N
XA9* J1
50
45
51
FLTH FROM CONT BITE CKTS
O
SHT 2
ISOLATOR
ISOLATOR
ISCLATOR
ISOLATOR
JAMH
FLTL
CM PULSE
WRMUPL
WRMUPL FROM SHEET 1
J1 XA9*
22
24
28
27
J2* P2
23
21
J1* P2
49
50

Figure 2-7. Synchronizer Processor Circuits (Sheet 3)

2-8. ANTENNA CONTROL CIRCUITS
(Figure 2-8)

The purpose of the antenna control circuits is to provide antenna switching information to the RF switch driver in the duplexer (see transmitting circuits). Antenna control requires two control parameters; antenna switch rate and antenna selection.

The ANTD (antenna drive) from the timing circuits controls switching rate and is applied to a flip-flop in the A7 card assembly as a clock pulse. This is the signal which causes the RF switch to connect the circulator in the duplexer between either of the antennas at the normal antenna switch rate. However, under certain conditions of operation, it may be required to stop antenna switching or to allow transmission or reception from one antenna to continue for an additional interval. This antenna selection mode is controlled by the APOSMSB and APOSLSB signals (Antenna Position Most/Least Significant Bit) generated by the microprocessor in the synchronizer processor circuits or by the test set.

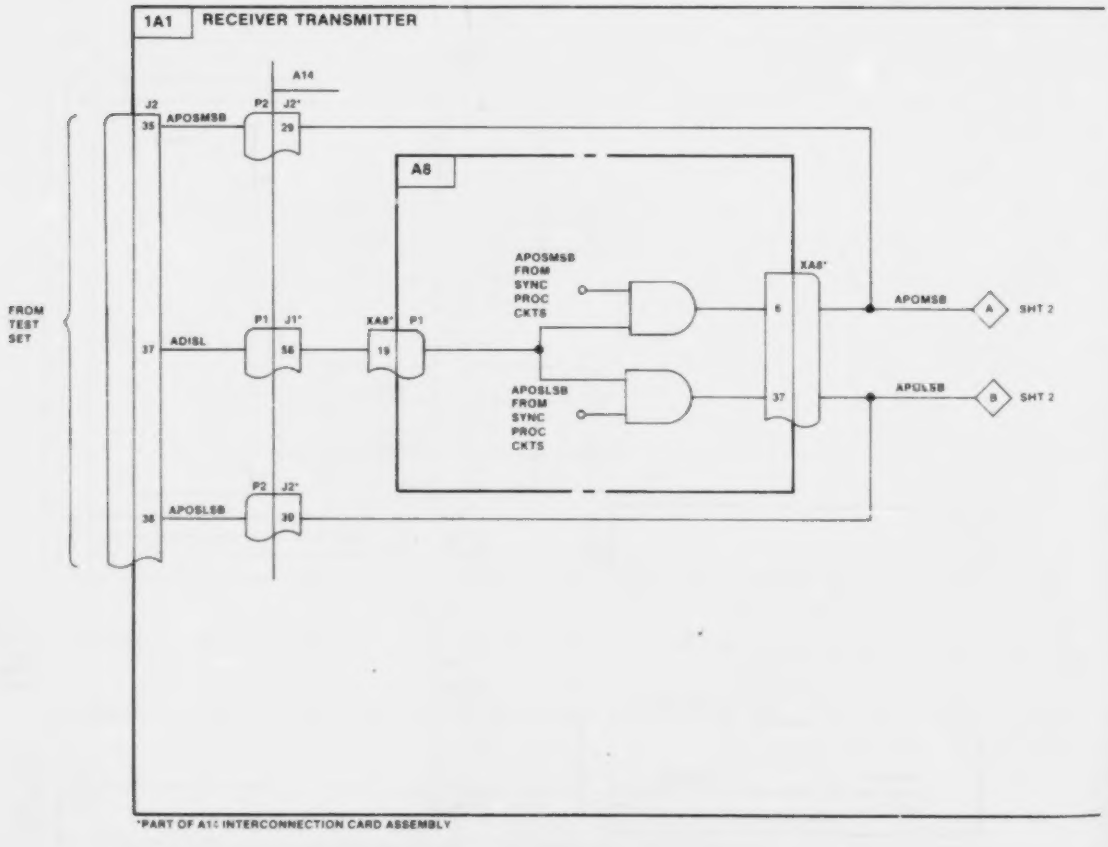
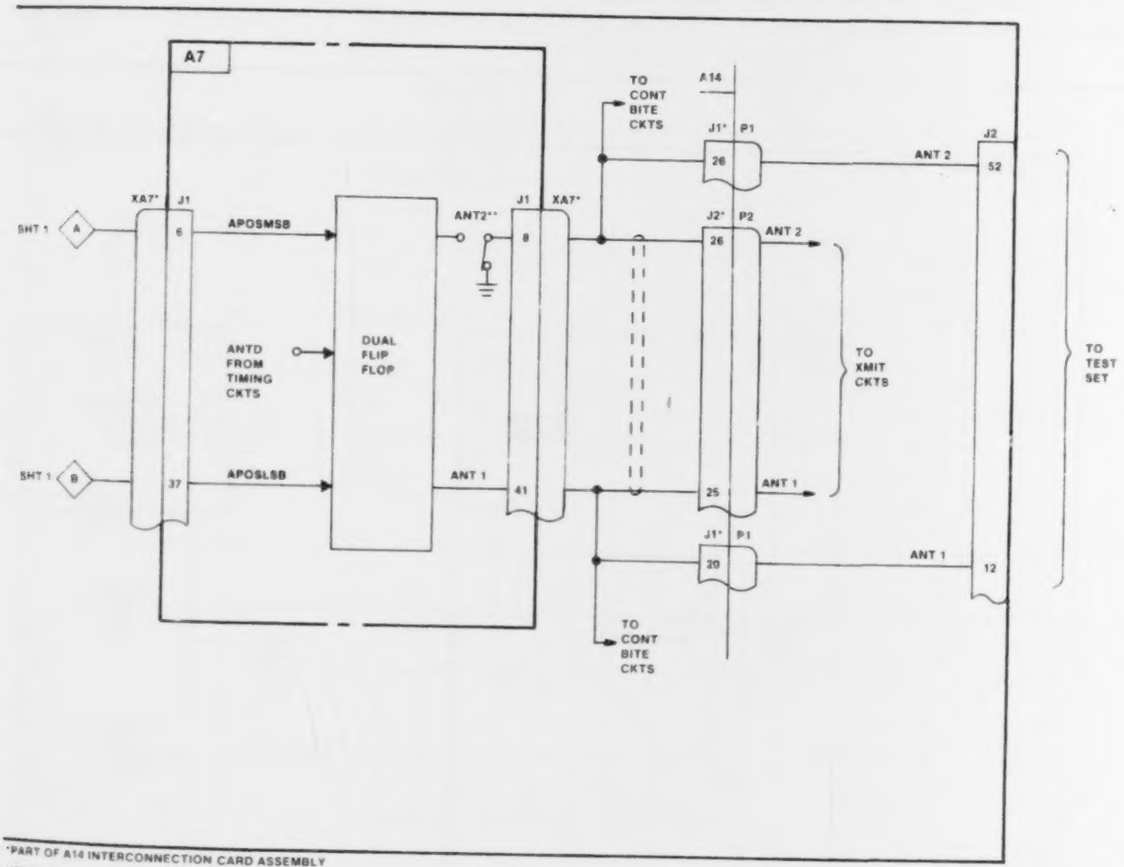

1A1
RECEIVER TRANSMITTER
A14
J2
P2
J2*
35
APOSMSB
29
A8
FROM TEST SET
APOSMSB FROM SYNC PROC CKTS
XA8*
6
APOMSB
A
SHT 2
P1
J1*
XA8*
P1
37
ADISL
56
19
APOSLSB FROM SYNC PROC CKTS
37
APOLSB
B
SHT 2
P2
J2*
38
APOSLSB
30
*PART OF A14 INTERCONNECTION CARD ASSEMBLY

Figure 2-8. Antenna Control Circuits (Sheet 1)

2-8. ANTENNA CONTROL CIRCUITS (Continued) (Figure 2-8)

The four binary combinations possible from these two logic signals would allow selection of four antenna positions, however only two are required for the (V)1 configuration of the countermeasures set. Thus, you will observe that the ANT 2 signal is wired to ground. Consequently, only the ANT 1 signal changes, thereby controlling antenna selection between two (V)1 configuration antennas.

During bench testing, the test set operator has the capability of selecting one of the antennas or allowing antenna switching at the normal rate. For the normal switch rate, the ADISL (antenna disable low) signal is high, and the synchronizer processor circuits APOSMSB, APOSLSB signals control antenna selection. When selecting one antenna only, the ADISL signal is active, thereby turning off the AND gates and allowing the APOSMSB/APOSLSB signals from the test set to control antenna selection.


A7
SHT 1
A
SHT 1
B
XA7*
J1
6
37
APOSMSB
APOSLSB
ANTD FROM TIMING CKTS
DUAL FLIP FLOP
ANT2**
ANT 1
J1
XA7*
8
41
TO CONT BITE CKTS
A14
J1*
P1
26
J2*
P2
26
25
ANT 2
ANT 1
TO XMIT CKTS
J1*
P1
20
TO CONT BITE CKTS
J2
ANT 2
52
ANT 1
12
TO TEST SET

*PART OF A14 INTERCONNECTION CARD ASSEMBLY

**TIED TO GROUND FOR V1 CONFIGURATION

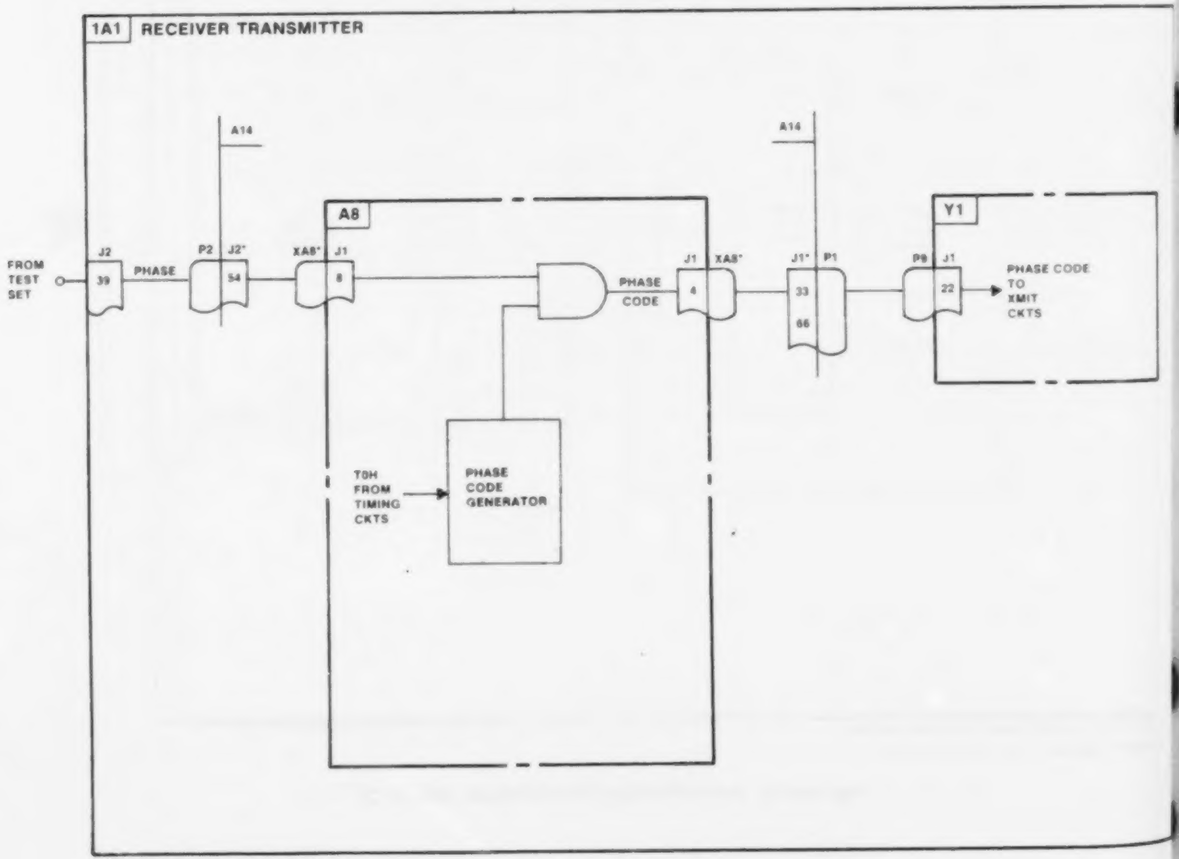
Figure 2-8. Antenna Control Circuits (Sheet 2)

2-9. PHASE CODE CIRCUITS
(Figure 2-9)

The function of the phase code circuits is to nullify ambiguous target signals. An ambiguous target is a real target located beyond the normal range of the system and therefore, of no interest. In any pulsed radar system, these real but unwanted target signals occur when an echo from a transmitted pulse returns after the next transmitted pulse has been sent. Thus, the target echo appears to be for a target within the range of system, when actually it is much further away. It is possible to receive ambiguous target returns resulting not only from the previous transmit pulse, but from others occurring even earlier.

A phase code generator on the A8 card of the RT produces a repetitive phase code which is routed to the FMO in the transmitting circuits. Here, the phase code modulates both the transmitting frequency F0 and the F1 first mixer frequency. Because both have the same phase modulation, the receiver will produce an output only for real targets within the normal range of the system and will discriminate against ambiguous targets.

Before being routed to the FMO, the phase code passes through an AND gate. This gate also receives a PHASE code input from the test set. Depending on the test mode selected, this input will be grounded, open or coded corresponding to OFF, NORMAL and TEST positions of the PHASE switch in the test set.


1A1
RECEIVER TRANSMITTER
A14
A14
A8
Y1
FROM TEST SET
J2
39
PHASE
P2
J2*
54
XA8*
J1
8
PHASE CODE
J1
XA8*
4
J1*
P1
33
66
P9
J1
22
PHASE CODE TO XMIT CKTS
T0H FROM TIMING CKTS
PHASE CODE GENERATOR

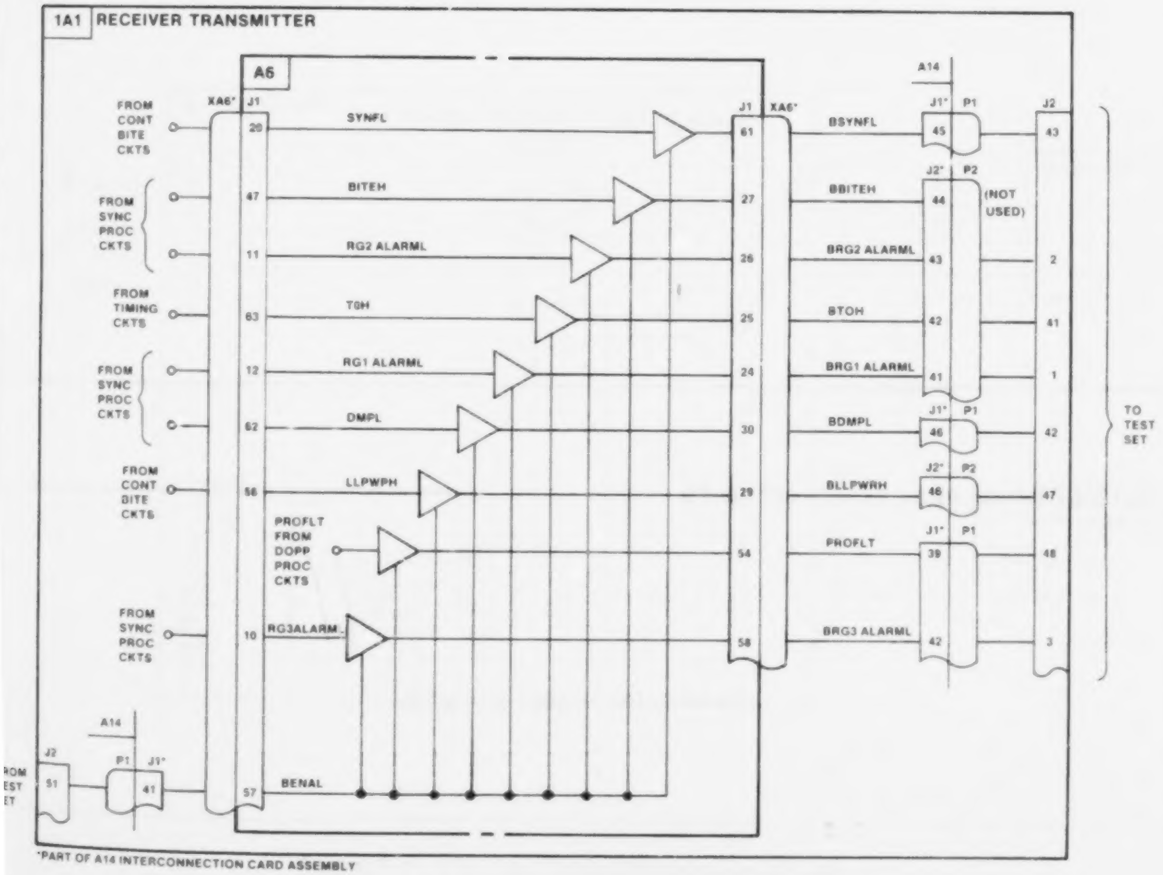
*PART OF A14 INTERCONNECTION CARD

Figure 2-9. Phase Code Circuits

2-10 TEST SET INTERFACE CIRCUITS (Figure 2-10)

The function of the test set interface circuits is to provide the test set with timing, fault and output signals generated within the RT. Each of the signals shown in the functional diagram pass through a buffer stage to provide isolation between the RT and test set. The BENAL (buffered enable low) signal is "low" and activates each of the buffer stages whenever the RT is connected to the test via cable W2.

The test set also receives other control and output signals from the RT. These are shown as part of the synchronizer processor circuits, antenna circuits, RT circuits, and antenna control circuits. Control inputs from the test set are described as part of the functional circuit to which they apply.


1A1
RECEIVER TRANSMITTER
A6
XA6*
J1
FROM CONT BITE CKTS
FROM SYNC PROC CKTS
FROM TIMING CKTS
FROM SYNC PROC CKTS
FROM CONT BITE CKTS
FROM SYNC PROC CKTS
20
47
11
63
12
62
56
10
57
SYNFL
BITEH
RG2 ALARML
TOH
RG1 ALARML
DMPL
LLPWPH
PROFLT FROM DOPP PROC CKTS
RG3ALARML
BENAL
J1
XA6*
61
27
26
25
24
30
29
54
58
BSYNFL
BBITEH
BRG2 ALARML
BTOH
BRG1 ALARML
BDMPL
BLLPWRH
PROFLT
BRG3 ALARML
A14
J1*
P1
45
J2*
P2
44
(NOT USED)
43
42
41
J1*
P1
46
J2*
P2
46
J1*
P1
39
42
J2
43
2
41
1
42
47
48
3
TO TEST SET
A14
J2
P1
J1*
51
41
ROM
EST
ET

*PART OF A14 INTERCONNECTION CARD ASSEMBLY

Figure 2-10. Test Set Interface Circuits

2-11 PERIODIC BITE CIRCUITS

(Refer to TM 11-5865-201-30-2)

2-12 INTERFERENCE MONITORING CIRCUITS

(Refer to TM 11-5865-201-30-2)

2-13 DOPPLER PROCESSOR CIRCUITS

(Refer to TM 11-5865-201-30-2)

2-14. 115 V AC POWER DISTRIBUTION CIRCUITS (Figure 2-11)

The countermeasures set receives 115 V ac, 3-phase, 400 Hz power from the aircraft bus on connector J1 of the power supply. Within the power supply it passes through contactor K1 to a three phase rectifier. Internal power supply circuits convert this primary power into regulated dc voltages required by the RT circuits.

The 115 V ac input is also used to power the three phase blower. Phase A energizes the elapsed time indicator which indicates elapsed RT operating time.

You will observe that contactor K1 is energized by +28 VS (switched) power applied to its coil terminals X1 and X2. This occurs when the control indicator power switch is placed its ON position. A thermal switch opens the +28-volt line if the power supply becomes overheated. The ground return for the contactor (terminal X2) is from a power control circuit in the power supply A3 card assembly. Should an overvoltage or overcurrent condition occur in any of the secondary power supplies, the power control opens the ground return thereby turning off the power supply.

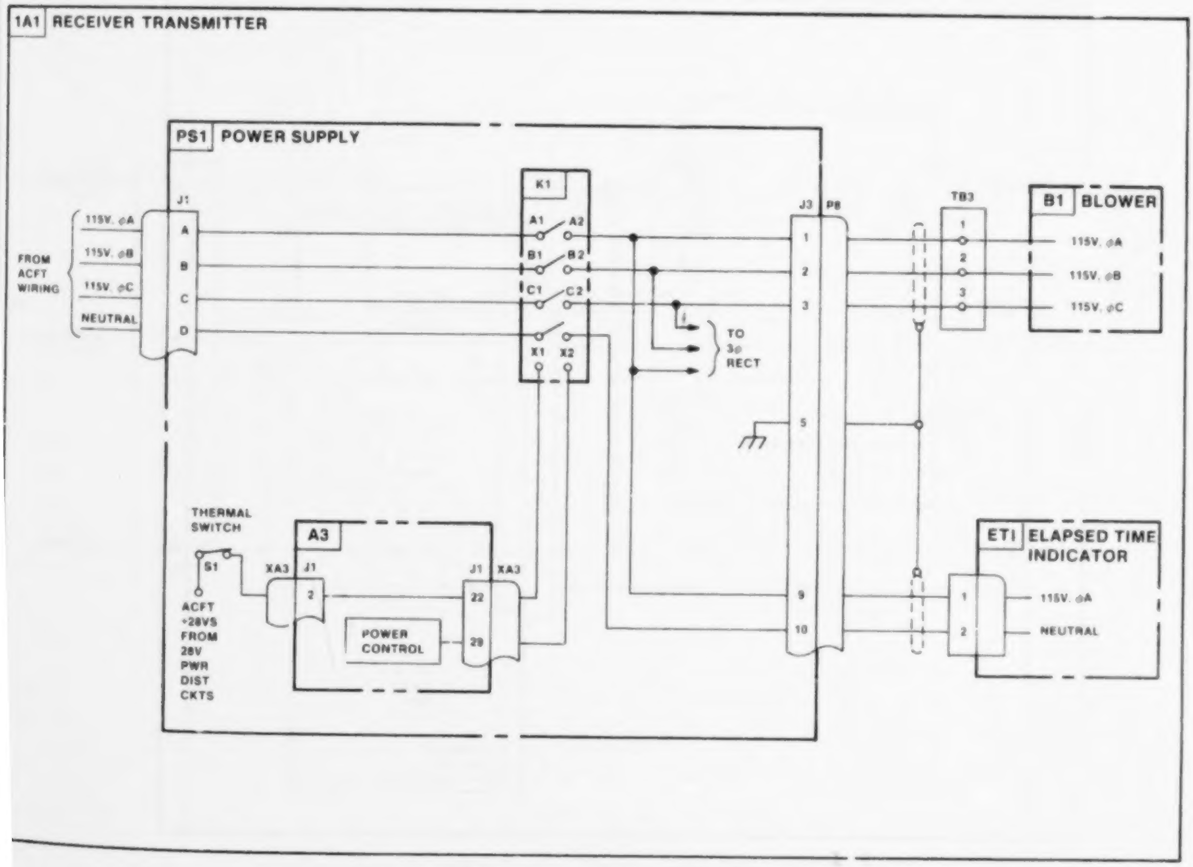

1A1 RECEIVER TRANSMITTER
PS1 POWER SUPPLY
FROM ACFT WIRING
115V. φA
115V. φB
115V. φC
NEUTRAL
J1
A
B
C
D
K1
A1
A2
B1
B2
C1
C2
X1
X2
TO 3φ RECT
J3
P8
1
2
3
5
9
10
TB3
1
2
3
B1 BLOWER
115V. φA
115V. φB
115V. φC
THERMAL SWITCH
S1
ACFT +28VS FROM 28V PWR DIST CKTS
A3
XA3
J1
2
J1
XA3
22
29
POWER CONTROL
ETI ELAPSED TIME INDICATOR
1
2
115V. φA
NEUTRAL

Figure 2-11. 115 V ac, Power Distribution Circuits

2-15. +28 V POWER DISTRIBUTION CIRCUITS (Figure 2-12)

Aircraft +28 V power is applied to the system on PS1 J1-J. From here it is routed out of the power supply to the POWER switch in control indicator. With the switch in the ON position, this voltage, +28 VS (+28 Volts Switched), is sent back to the power supply in the RT where it is used to energize the 115 Vac contactor.

The +28 VS also causes relay K1 in the A19 CM heat assembly to energize. The relay contacts connect regulated +24 V to a frequency-stabilizing oven in the FMO (refer to +24 V power distribution units). When the POWER switch is in the OFF position, the normally closed relay contacts of K1 connect a +24 V regulator in the A19 assembly to the FMO oven. The +24 V regulator receives +28 V input power (CM HEAT) whenever the preheat mode is selected.

The +28 VS also lights the STBY indicator whenever the PUSH FOR STANDBY switch is depressed. With the switch in this position, the PAON signal (ground) is disabled causing the system to go into the standby mode.

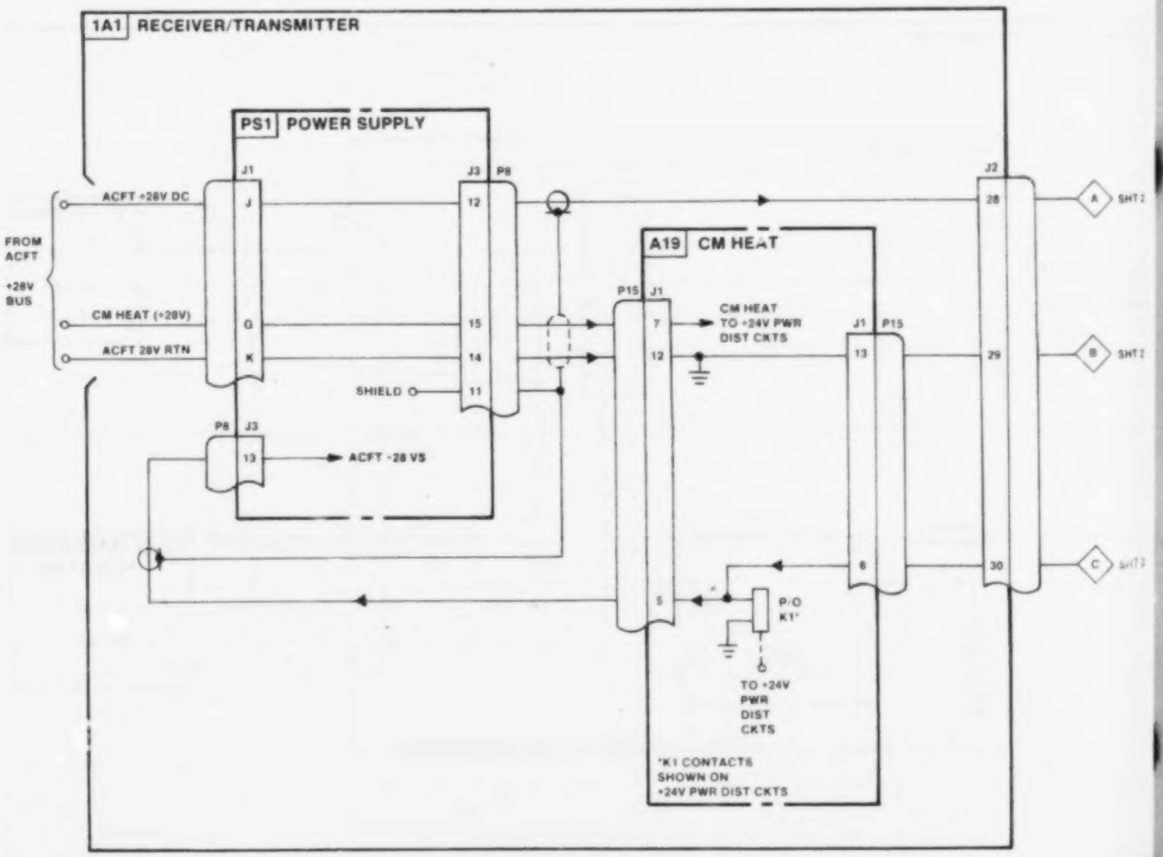

1A1 RECEIVER/TRANSMITTER
PS1 POWER SUPPLY
FROM ACFT
+28V BUS
ACFT +28V DC
CM HEAT (+28V)
ACFT 28V RTN
J1
J
G
K
J3
P8
12
15
14
11
SHIELD
P8
J3
13
ACFT +28 VS
A19 CM HEAT
P15
J1
7
12
5
CM HEAT TO +24V PWR DIST CKTS
J1
P15
13
6
P/O K1*
TO +24V PWR DIST CKTS
*K1 CONTACTS SHOWN ON +24V PWR DIST CKTS
J2
28
29
30
A
SHT 2
B
SHT 2
C
SHT 2

Figure 2-12. +28 V Power Distribution Circuits (Sheet 1)

2-15. +28 V POWER DISTRIBUTION CIRCUITS (Continued) (Figure 2-12)

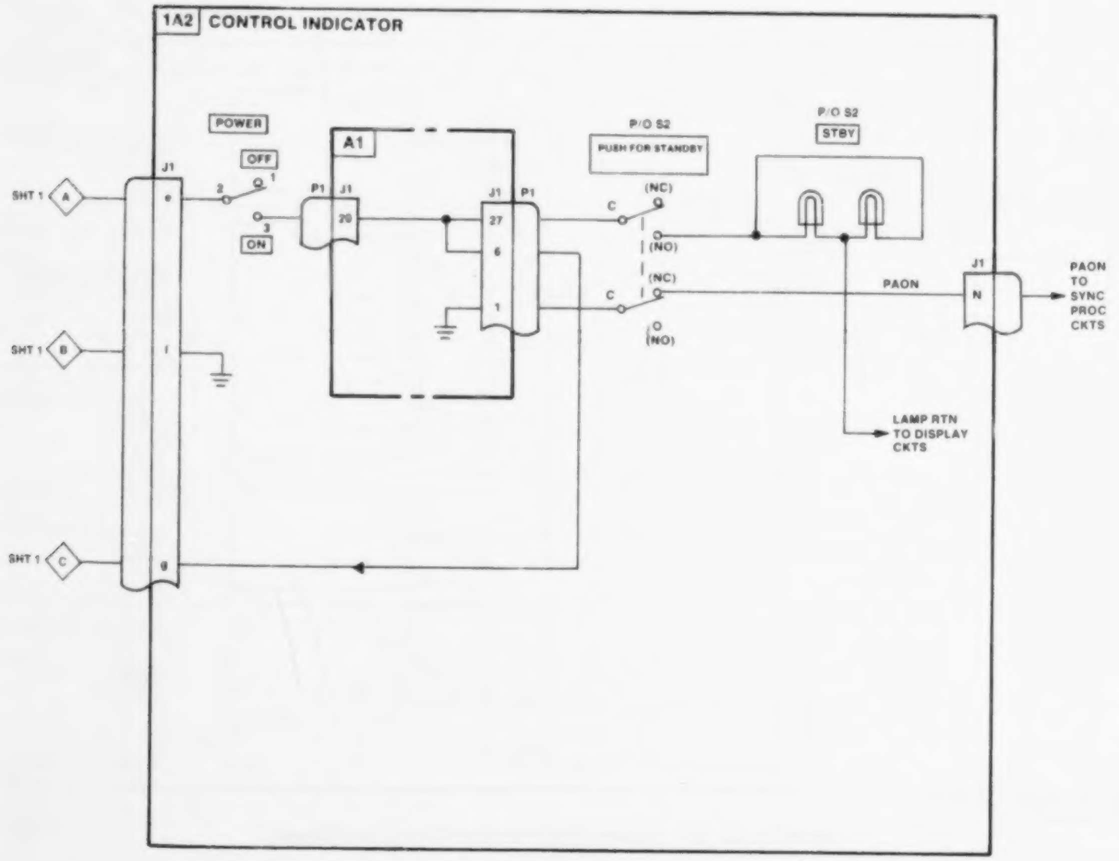
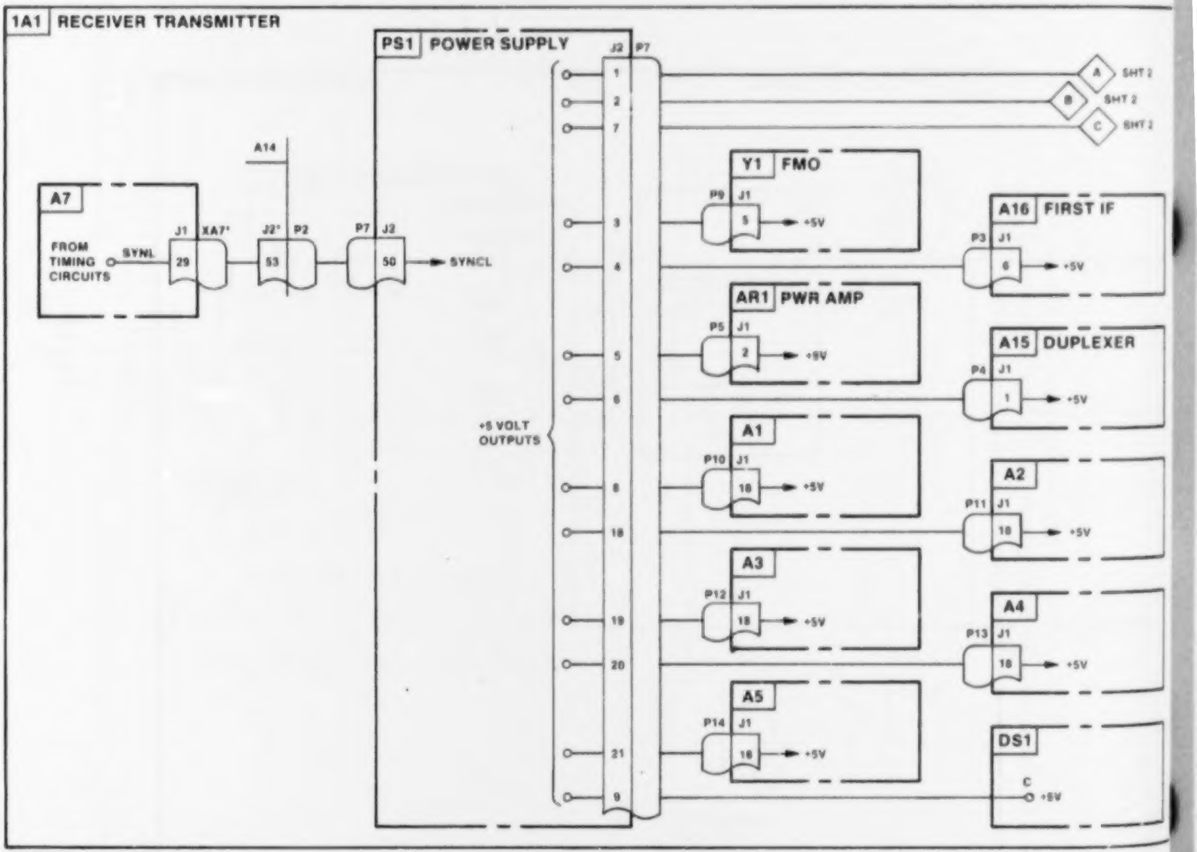

1A2
CONTROL INDICATOR
POWER
OFF
ON
J1
SHT 1 A
SHT 1 B
SHT 1 C
e
f
g
1
2
3
A1
P1
J1
20
J1
P1
27
6
1
P/O S2
PUSH FOR STANDBY
P/O S2
STBY
C
(NC)
(NO)
C
(NC)
(NO)
PAON
J1
N
PAON TO SYNC PROC CKTS
LAMP RTN TO DISPLAY CKTS

Figure 2-12. +28 V Power Distribution Circuits (Sheet 2)

2-16. +5 V POWER DISTRIBUTION CIRCUITS (Figure 2-13)

The regulated +5 volt power generated in the power supply is distributed to all circuit cards in the receiver transmitter as well as to the FMO, first IF, duplexer, and power amplifier. It is also used to drive the VSWR fault indicator DS1. When the receiver transmitter is connected to the test set, the +5 V may be monitored at the test set METER jacks.

The +5 V power, as well as the other dc outputs of the power supply, are derived from an inverter synchronized to the PRF of the system. The SYNCL signal from the timing circuits provides inverter synchronization, and the inverter input is the rectified 115 V, 400 Hz, 3ϕ input power.

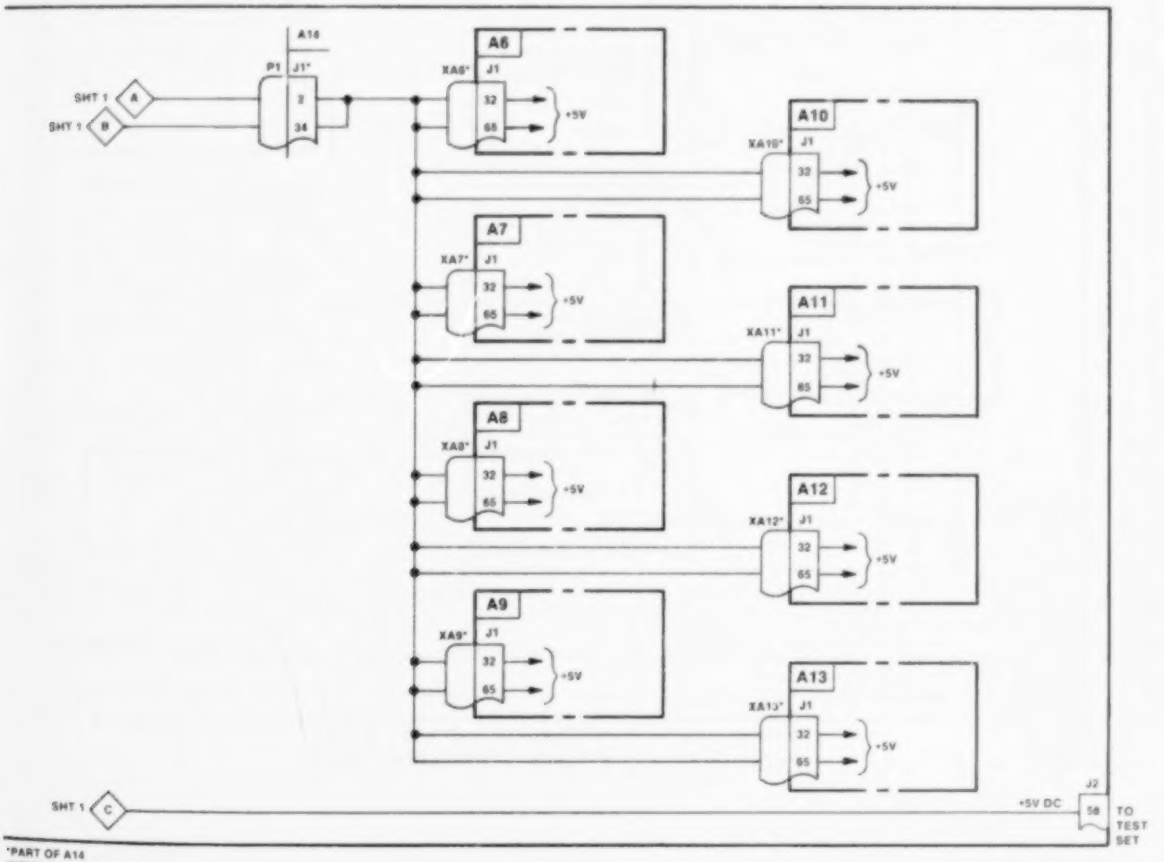


1A1 RECEIVER TRANSMITTER
PS1 POWER SUPPLY
J2
P7
1
2
7
A SHT 2
B SHT 2
C SHT 2
A14
A7
FROM TIMING CIRCUITS
SYNL
J1
XA7*
29
J2*
P2
53
P7
J2
50
SYNCL
3
4
5
6
8
18
19
20
21
9
+5 VOLT OUTPUTS
Y1 FMO
P9
J1
5
+5V
A16 FIRST IF
P3
J1
6
+5V
AR1 PWR AMP
P5
J1
2
+5V
A15 DUPLEXER
P4
J1
1
+5V
A1
P10
J1
18
+5V
A2
P11
J1
18
+5V
A3
P12
J1
18
+5V
A4
P13
J1
18
+5V
A5
P14
J1
18
+5V
DS1
C
+5V

*PART OF A14 INTERCONENCTION CARD ASSEMBLY

Figure 2-13. +5 V Power Distribution Circuits (Sheet 1)

2-16. +5 V POWER DISTRIBUTION CIRCUITS (Continued) (Figure 2-13)

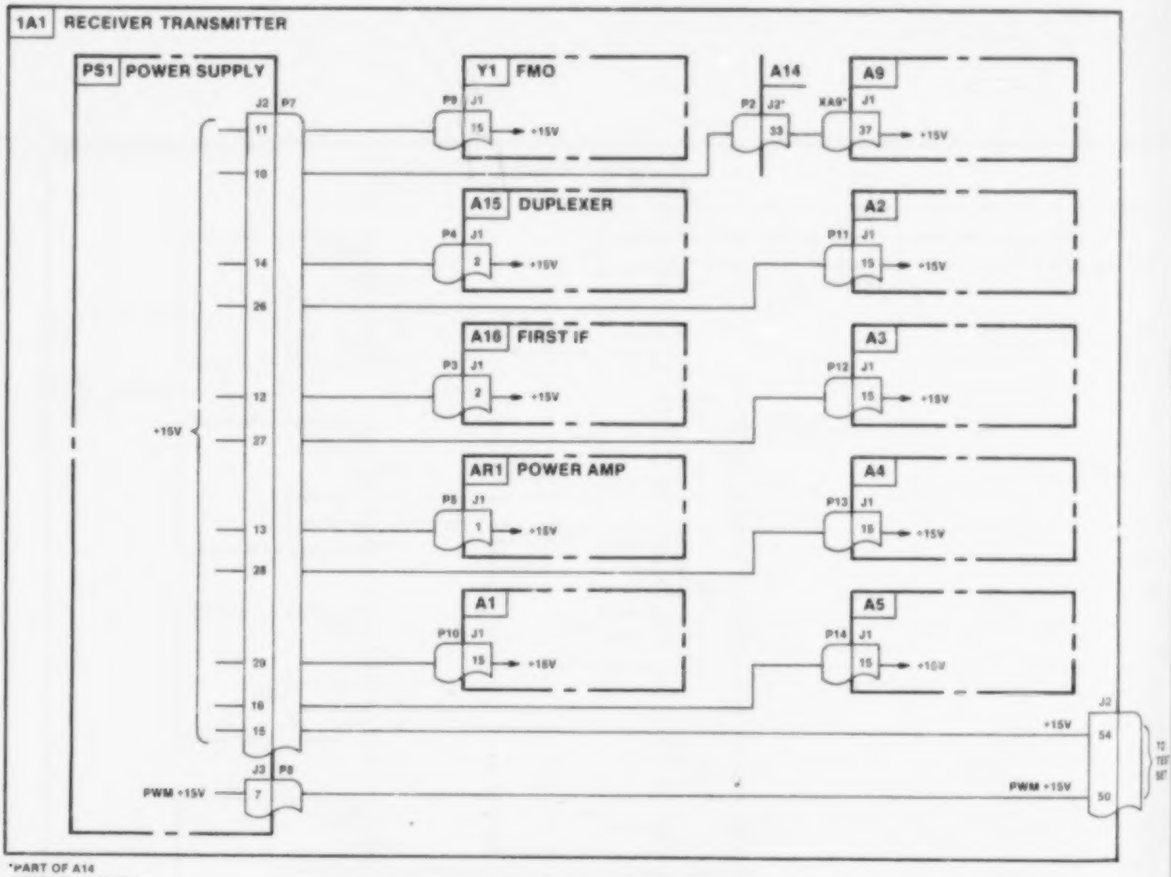

A14
P1
J1*
SHT 1
A
SHT 1
B
2
34
A6
XA6*
J1
32
65
+5V
A10
XA10*
J1
32
65
+5V
A7
XA7*
J1
32
65
+5V
A11
XA11*
J1
32
65
+5V
A8
XA8*
J1
32
65
+5V
A12
XA12*
J1
32
65
+5V
A9
XA9*
J1
32
65
+5V
A13
XA13*
J1
32
65
+5V
J2
SHT 1
C
+5V DC
58
TO TEST SET

*PART OF A14
INTERCONNECTION CARD
ASSEMBLY

Figure 2-13. +5 V Power Distribution Circuits (Sheet 2)

2-17. +15 V POWER DISTRIBUTION CIRCUITS (Figure 2-14)

The +15 V output of the power supply is distributed to the FMO, duplexer, power amplifier, first IF, and each of the second IF card assemblies. This voltage is also made available to the test set for monitoring as is the PWM +15 V generated separately within the power supply.


1A1 RECEIVER TRANSMITTER
PS1 POWER SUPPLY
J2
P7
11
10
14
26
12
27
13
28
29
16
15
+15V
J3
P8
7
PWM +15V
Y1 FMO
P9
J1
15
+15V
A15 DUPLEXER
P4
J1
2
+15V
A16 FIRST IF
P3
J1
2
+15V
AR1 POWER AMP
P5
J1
1
+15V
A1
P10
J1
15
+15V
A14
P2
J2*
33
A9
XA9*
J1
37
+15V
A2
P11
J1
15
+15V
A3
P12
J1
15
+15V
A4
P13
J1
15
+15V
A5
P14
J1
15
+15V
J2
+15V
54
PWM +15V
50
TO TEST SET

*PART OF A14 INTERCONNECTION CARD ASSEMBLY

Figure 2-14. +15 V Power Distribution Circuits

2-18. -15 V POWER DISTRIBUTION CIRCUITS (Figure 2-15)

The -15 V output of the power supply is distributed to the all second IF circuit cards, the power amplifier, first IF and FMO assemblies. This voltage is also made available to the test set for monitoring.

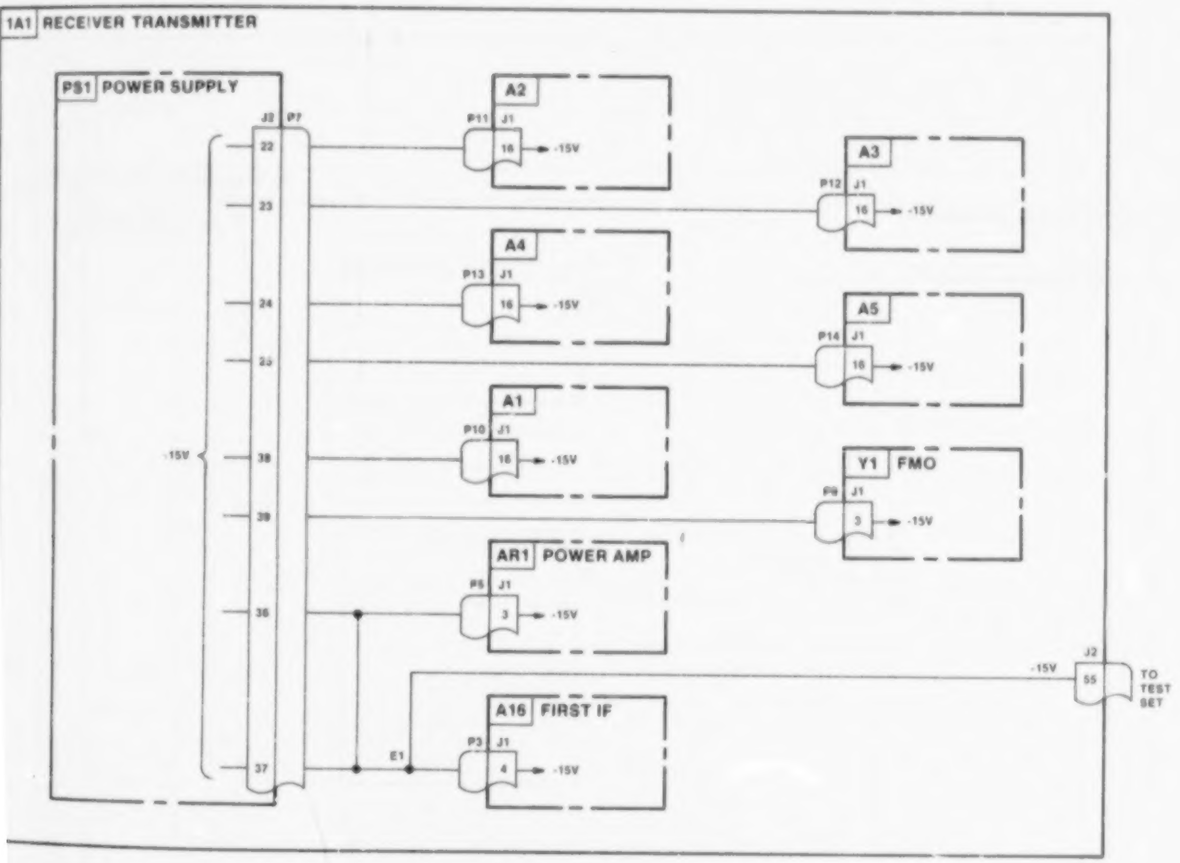

1A1 RECEIVER TRANSMITTER
PS1 POWER SUPPLY
J2
P7
22
23
24
25
38
39
36
37
-15V
A2
P11
J1
16
-15V
A3
P12
J1
16
-15V
A4
P13
J1
16
-15V
A5
P14
J1
16
-15V
A1
P10
J1
16
-15V
Y1 FMO
P9
J1
3
-15V
AR1 POWER AMP
P5
J1
3
-15V
A16 FIRST IF
P3
J1
4
-15V
E1
-15V
J2
55
TO TEST SET

Figure 2-15. -15 V Power Distribution Circuits

2-19. -8 V AND +32 V POWER DISTRIBUTION CIRCUITS (Figure 2-16)

The -8 V power produced in the power supply is used only by the FMO, and the +32 V power is used only by the power amplifier. Both voltages are connected to RT J2 so that they can be monitored by the test set.

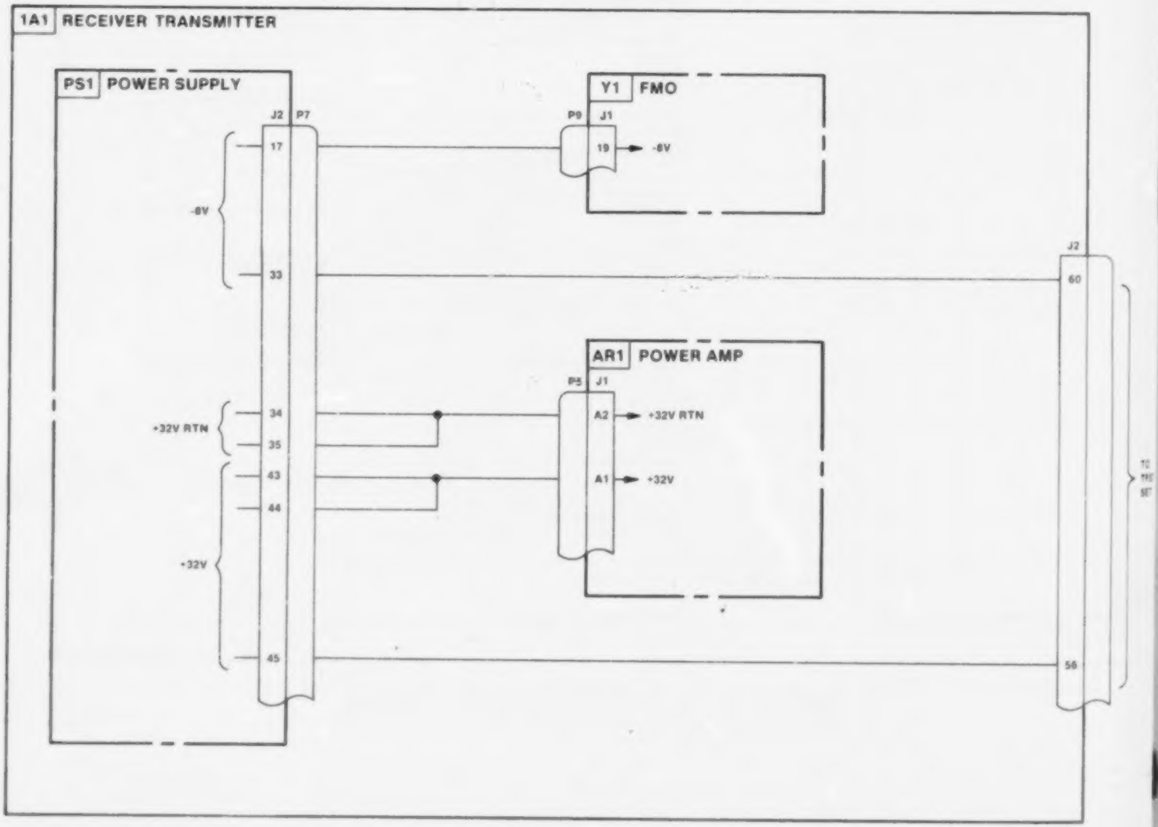

1A1 RECEIVER TRANSMITTER
PS1 POWER SUPPLY
J2
P7
17
-8V
33
+32V RTN
34
35
43
44
+32V
45
Y1 FMO
P9
J1
19
-8V
AR1 POWER AMP
P5
J1
A2
+32V RTN
A1
+32V
J2
60
56
TO
TE
SET

Figure 2-16. -8 V and +32 V Power Distribution Circuits

pages tightly bound

2-20. +24 V AND -45 V POWER DISTRIBUTION CIRCUITS (Figure 2-17)

The +24 V power produced in the power supply is used only in the FMO. One +24 V line passes through the contacts of the energized K1 relay in the CM heat assembly to the crystal oven in the FMO. The other line is applied to other circuitry in the FMO. If relay K1 is not energized (system turned-off) the FMO oven is connected to a +24 V regulator in the CM heat assembly through the normally-closed contacts of K1. If an oven preheat mode is required, aircraft +28 V power (CM HEAT) energizes the regulator allowing the oven to heat without any other circuits in the system to be activated (see also +28 V power distribution circuits). The +28 V power is also connected to RT connector J2 so that it can be monitored in the test set.

The -45 V power produced in the power supply is used only in the duplexer. It is also connected to RT connector J2 so that it can be monitored in the test set.

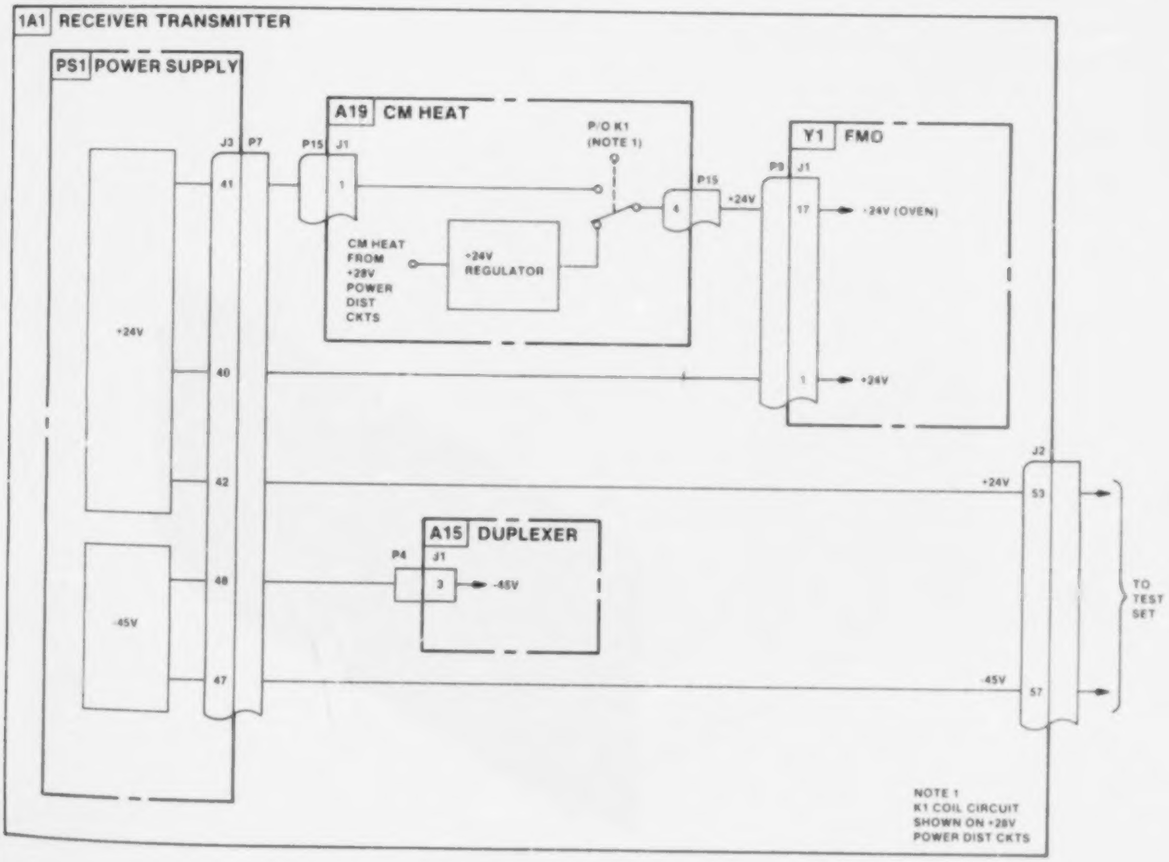

1A1 RECEIVER TRANSMITTER
PS1 POWER SUPPLY
+24V
-45V
J3
P7
41
40
42
48
47
A19 CM HEAT
P15
J1
1
P/O K1
(NOTE 1)
CM HEAT
FROM
+28V
POWER
DIST
CKTS
+24V
REGULATOR
P15
4
+24V
Y1 FMO
P9
J1
17
+24V (OVEN)
1
+24V
J2
+24V
53
A15 DUPLEXER
P4
J1
3
-45V
-45V
57
TO
TEST
SET
NOTE 1
K1 COIL CIRCUIT
SHOWN ON +28V
POWER DIST CKTS

Figure 2-17. +24 V and -45 V Power Distribution Circuits

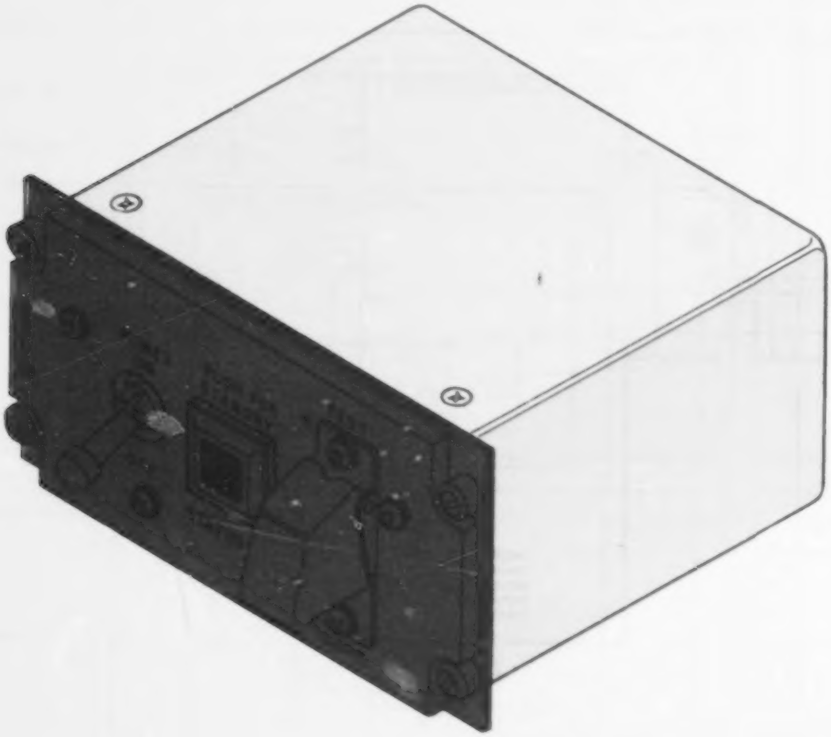
SECTION II.
CONTROL INDICATOR OPERATION

SECTION CONTENTS **PAGE**

PURPOSE AND USE 2-35
CONTROL CIRCUITS 2-36
INTERFACE CIRCUITS 2-37

2-21. PURPOSE AND USE

The purpose of the control indicator is to provide the operator with control of the two modes of operation (standby and on) and to display system status. The control indicator also relays receiver transmitter status signals (JAM or INOP) to the aircraft master caution panel and the CM (countermeasures) signal to the M-130 flare dispenser. A FLARE TEST switch on the unit provides for testing system interface with the M-130 system.



2-22. CONTROL CIRCUITS
(Figure 2-18)

When the POWER switch is placed in the ON position, aircraft +28 volts from the receiver transmitter is applied back to the receiver transmitter activating its power supply. The WRMUPL (warm-up low) signal will provide a ground return path from relay K1, which will energize lighting the WRMUP lamp. After approximately 10 minutes, the FMO will have achieved warm-up, and the WRMUP signal will go high causing K1 to release and the WRMUP indicator to go out. This informs the operator that the system is now operating.

If the PUSH FOR STANDBY switch is depressed, the STBY indicator is energized and the PA ON ground to the receiver transmitter is removed. This inhibits the power amplifier in the receiver transmitter, while allowing all other receiver transmitter circuits to remain activated (standby mode). You will note that the ground return for both the STBY and WRMUP indicators is obtained from the control indicator interface circuits. As will be described, this permits control of the brightness of these two indicators.

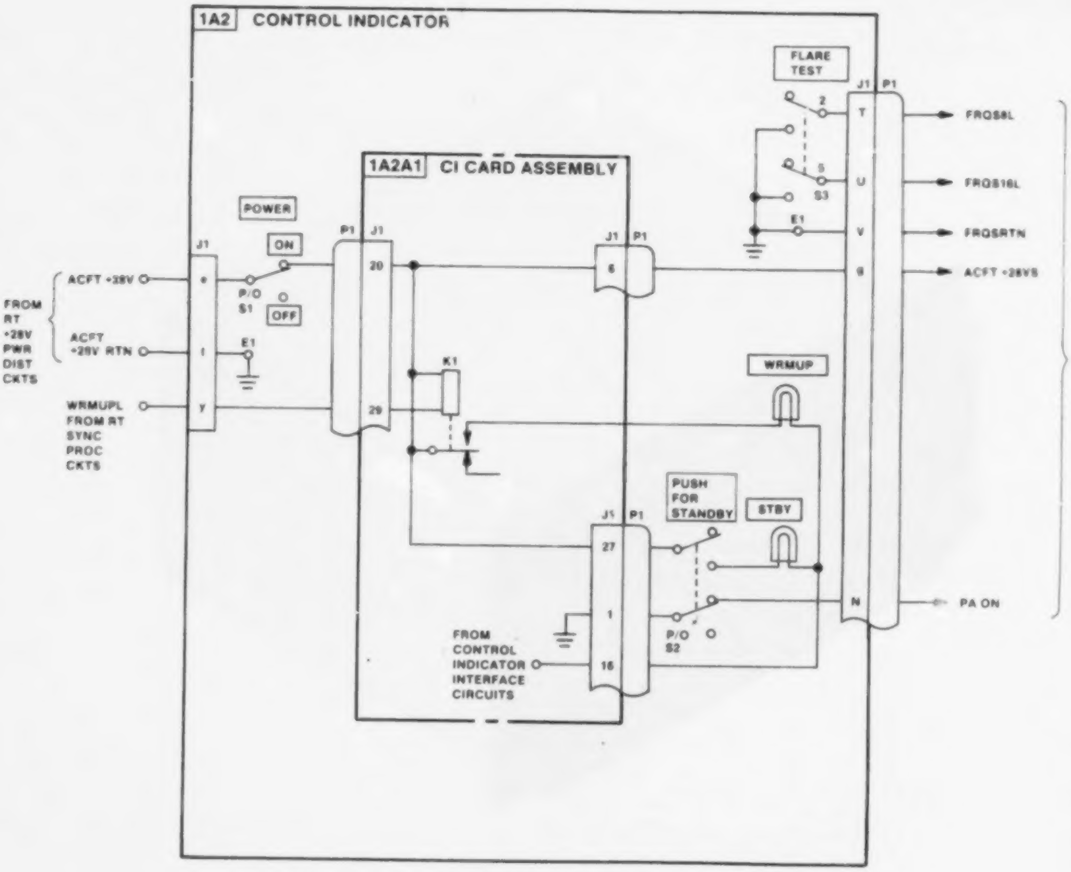

1A2 CONTROL INDICATOR
1A2A1 CI CARD ASSEMBLY
FLARE TEST
2
5
S3
E1
J1
P1
T
U
V
8
FRQS8L
FRQS16L
FRQSRTN
ACFT +28VS
POWER
ON
OFF
P/O S1
ACFT +28V
FROM RT +28V PWR DIST CKTS
ACFT +28V RTN
e
f
y
WRMUPL FROM RT SYNC PROC CKTS
20
29
6
K1
WRMUP
PUSH FOR STANDBY
STBY
27
1
16
P/O S2
N
PA ON
TO RT SYNC PROC CKTS
FROM CONTROL INDICATOR INTERFACE CIRCUITS

Figure 2-18. Control Indicator Control Circuits

2-23. INTERFACE CIRCUITS (Figure 2-19)

The control indicator receives three status signals from the receiver transmitter: FAULT, JAMH (Jam High) and CM PULSE.

The FAULT and JAMH signals turn on transistor drivers which energize relays K2 and K3, opening normally closed contacts. This causes CM INOP or CM JAM indicators on the aircraft master caution panel to light alerting the operator to the presence of jamming or countermeasures set inoperation.

The CM PULSE input from the RT occurs when the system has detected a target. This signal is buffered in an optical isolator and is sent to the M-130 system for flare ejection. Both positive and negative flare ejection signals are available.

As mentioned earlier, the brightness of the STBY and WRMUP indicator is controllable. If the DIML (dim low) signal is present (which occurs when the operator selects a lower intensity for aircraft instrument illumination), the ground return for the lamps is through a zener diode which lowers the voltage applied to the indicator lamps. When the DIML signal is not present, a transistor shunts the zener, allowing the full voltage to be applied to the indicators.

The front panel engraving on the control indicator is illuminated by lamps within the edge lit front panel; these lamps operate on 0 to 5 volts ac from the aircraft cockpit lighting system.

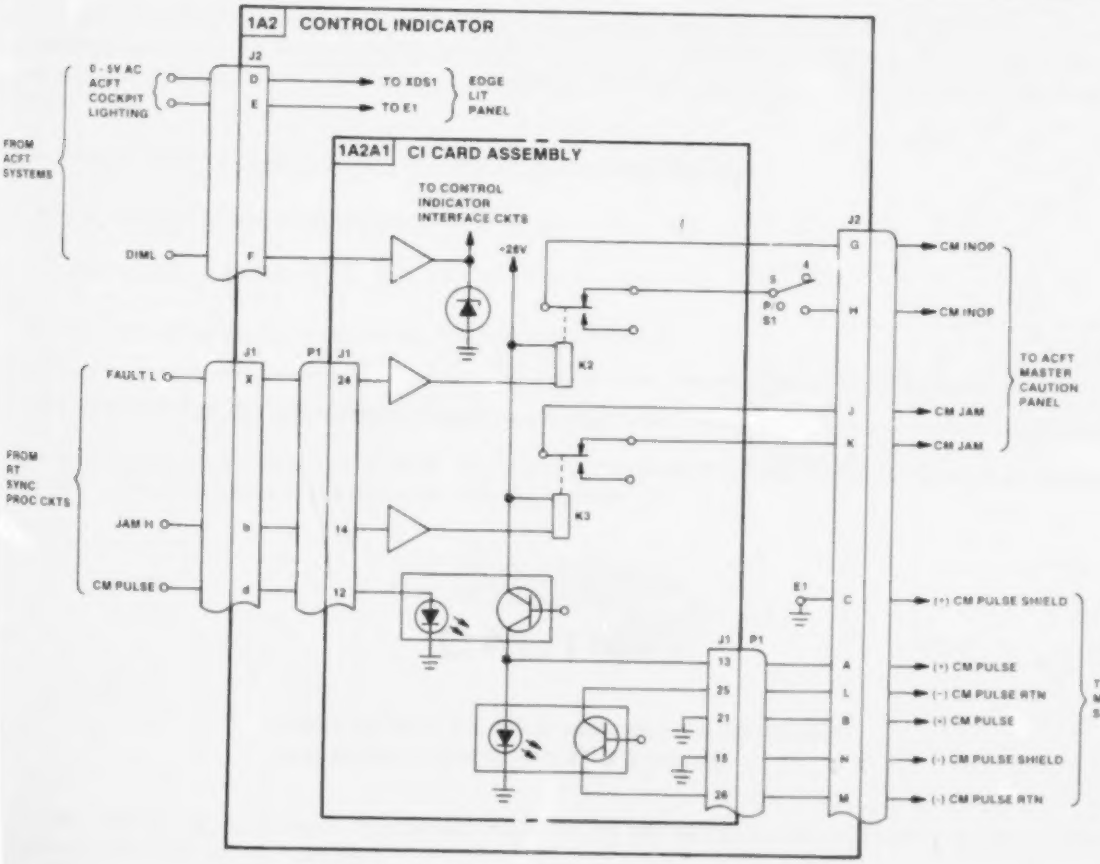

1A2 CONTROL INDICATOR
J2
0 - 5V AC
ACFT
COCKPIT
LIGHTING
D
E
TO XDS1
TO E1
EDGE
LIT
PANEL
FROM
ACFT
SYSTEMS
1A2A1 CI CARD ASSEMBLY
TO CONTROL
INDICATOR
INTERFACE CKTS
+28V
DIML
F
J2
G
CM INOP
5
4
P/O
S1
H
CM INOP
J1
P1
J1
FAULT L
X
24
K2
TO ACFT
MASTER
CAUTION
PANEL
J
CM JAM
K
CM JAM
FROM
RT
SYNC
PROC CKTS
JAM H
b
14
K3
CM PULSE
d
12
E1
C
(+) CM PULSE SHIELD
J1
P1
13
A
(+) CM PULSE
25
L
(-) CM PULSE RTN
21
B
(+) CM PULSE
TO
M-130
SYSTEM
15
N
(-) CM PULSE SHIELD
26
M
(-) CM PULSE RTN

Figure 2-19. Control Indicator Interface Circuits

CHAPTER 3
MAINTENANCE INSTRUCTIONS FOR RECEIVER TRANSMITTER

SECTION I.
RECEIVER TRANSMITTER CHECK PROCEDURE

SECTION CONTENTS **PAGE**

GENERAL 3-1
TEST SETUP INTERCONNECTIONS 3-1
INITIAL SWITCH POSITIONS 3-3
TEST PROCEDURE 3-3

3-1. GENERAL

This section contains a check procedure which will permit you to determine if the receiver transmitter is operating correctly. To test a receiver transmitter, you will be required to connect it into a test setup using the test set and other standard test equipment. You should perform a receiver transmitter check when:

- You receive a suspected defective unit from unit maintenance.
- You receive a new system from army supply.
- After repair of a unit.
- Anytime you suspect a unit is not functioning properly.

3-2. TEST SETUP INTERCONNECTIONS

Remove cover from the receiver transmitter. Connect the receiver transmitter to the test set as shown in figure 3-1 using the test cables supplied with the test set.

CAUTION

Ensure that the 115 V, 400 Hz power source is not activated when connecting power cable W1 to the test set.

Connect the scope, multimeter, and power meter to the test set as shown in figure 3-2 using general purpose test leads and RF cables.

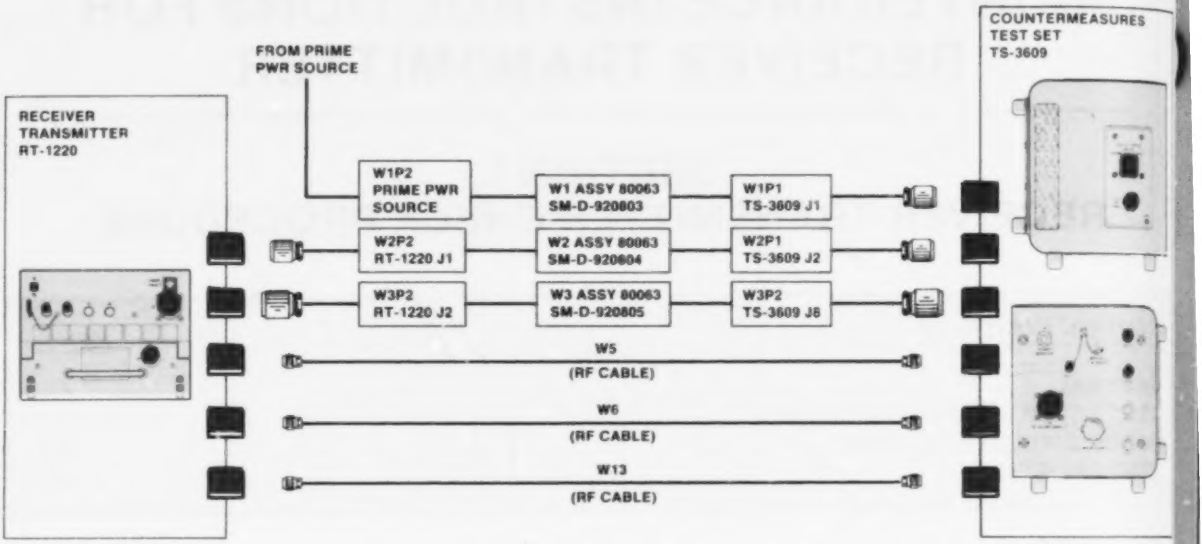

FROM PRIME
PWR SOURCE
RECEIVER
TRANSMITTER
RT-1220
COUNTERMEASURES
TEST SET
TS-3609
W1P2
PRIME PWR
SOURCE
W1 ASSY 80063
SM-D-920803
W1P1
TS-3609 J1
W2P2
RT-1220 J1
W2 ASSY 80063
SM-D-920804
W2P1
TS-3609 J2
W3P2
RT-1220 J2
W3 ASSY 80063
SM-D-920805
W3P2
TS-3609 J8
W5
(RF CABLE)
W6
(RF CABLE)
W13
(RF CABLE)

Figure 3-1. Receiver Transmitter and Test Set Interconnections

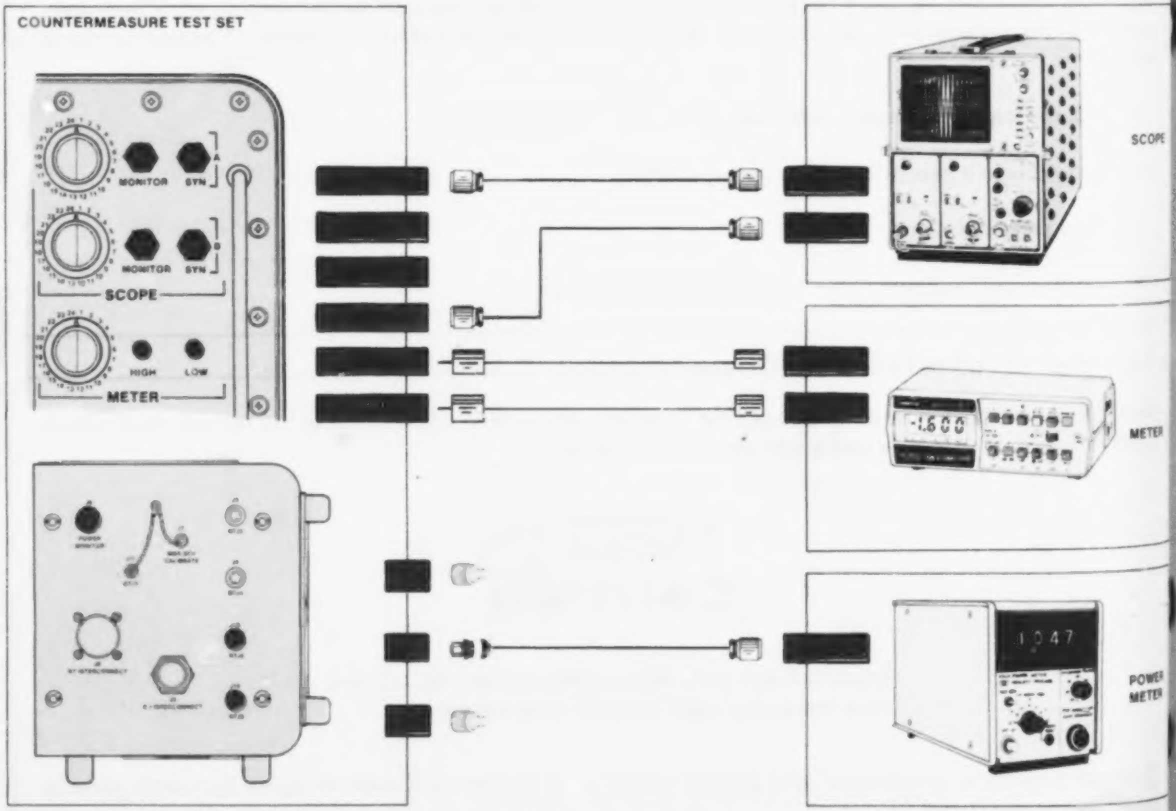
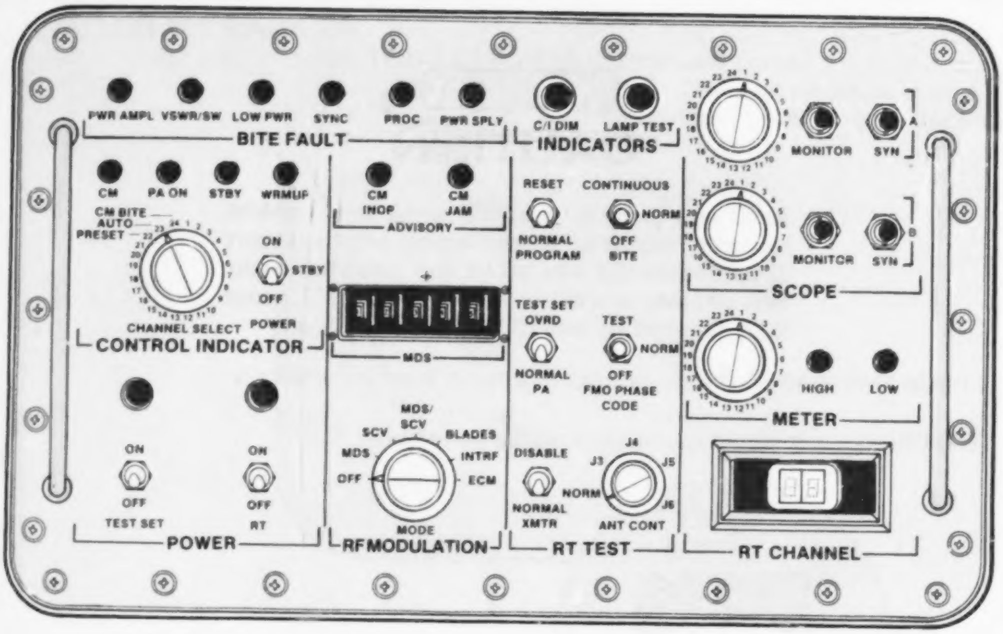

COUNTERMEASURE TEST SET
MONITOR
SYN
A
MONITOR
SYN
B
SCOPE
HIGH
LOW
METER
SCOPE
METER
POWER
METER

Figure 3-2. Test Set and Monitoring Equipment Interconnections

3-3. INITIAL SWITCH POSITIONS

Set the switches on the test set to their OFF, NORM (NORMAL), fully counterclockwise or lowest numbered positions, except for the CONTROL INDICATOR CHANNEL SELECT switch, which you set to position AUTO. Set the BITE and FMO PHASE CODE switches to the NORM position.


PWR AMPL
VSWR/SW
LOW PWR
SYNC
PROC
PWR SPLY
BITE FAULT
C/I DIM
LAMP TEST
INDICATORS
CM
PA ON
STBY
WRMUP
CM BITE
AUTO
PRESET
CHANNEL SELECT
ON
STBY
OFF
POWER
CONTROL INDICATOR
CM INOP
CM JAM
ADVISORY
MDS
RESET
NORMAL PROGRAM
CONTINUOUS
NORM
OFF BITE
TEST SET OVRD
NORMAL PA
TEST
NORM
OFF FMO PHASE CODE
MONITOR
SYN
A
MONITOR
SYN
B
SCOPE
HIGH
LOW
METER
ON
OFF
TEST SET
ON
OFF
RT
POWER
MDS/SCV
SCV
MDS
OFF
BLADES
INTRF
ECM
MODE
RF MODULATION
DISABLE
NORMAL XMTR
J3
J4
J5
J6
NORM
ANT CONT
RT TEST
RT CHANNEL

Set the power switches on the standard test equipment to "on" so that this equipment will warm up.

3-4. TEST PROCEDURE

Check the receiver transmitter by performing the steps listed in the OPERATION column of the following chart. If you do not obtain the results specified in the NORMAL INDICATION column, refer to the CORRECTIVE ACTION column for instructions. The CORRECTIVE ACTION column will refer you to a possible cause for the not obtaining the normal indication. Usually this will be an assembly of the transmitter. If a FAULT NUMBER is listed, refer to the troubleshooting table in paragraph 3-10, Section II for a troubleshooting procedure to help you isolate the malfunction to a specific RT assembly.

When the CORRECTIVE ACTION column directs you to the synchronizer or doppler processor, use the maintenance assistance module (MAM) to locate a specific circuit card within these units. Refer to Section II, paragraph 3-6 and 3-7, for a description and use of the MAM.

If after performing the corrective action, you are still unable to obtain the normal indication(s), refer to the functional schematic diagrams and associated circuit descriptions given in Chapter 2. Use the ohmmeter to check wiring associated with the problem you are experiencing, and repair the wiring if required. Read the circuit description as it will help you understand the relationships among the several functional subsystems of the receiver transmitter and may aid you in locating a defective component.

f you cannot correct the problem, return the receiver transmitter to a higher category of maintenance for repair.

3.4 TEST PROCEDURES (Continued)

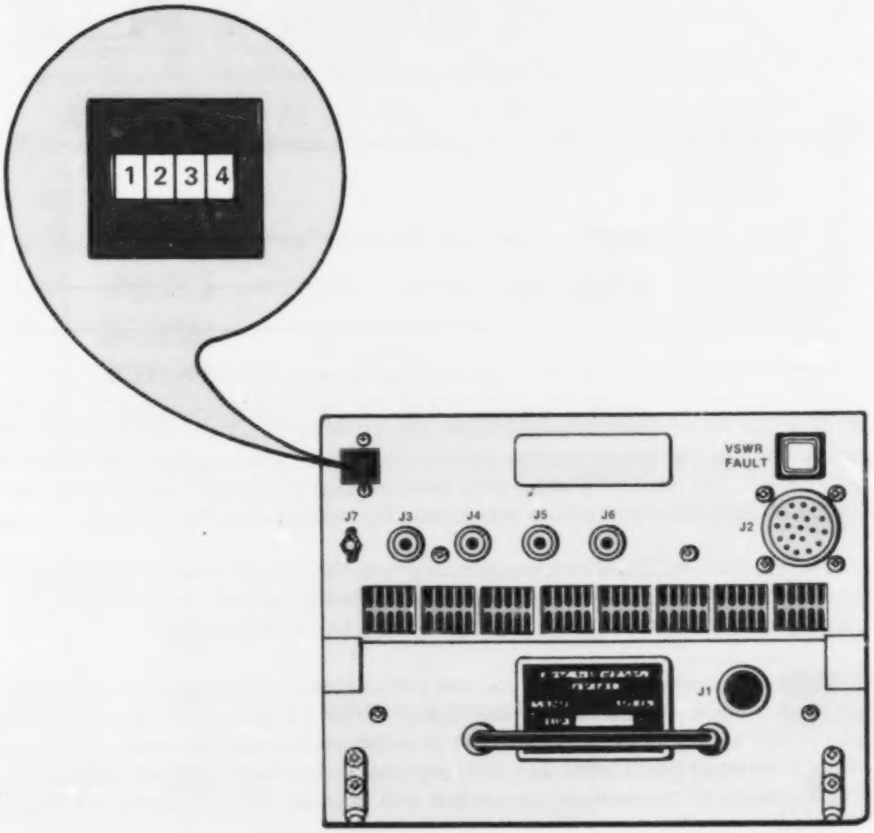
STEP	OPERATION → NORMAL INDICATION → CORRECTIVE ACTION

CAUTION

Do not apply power to the RT with circuit card assemblies removed or without the duplexer antenna output connectors J3 and J4 connected to the test set. Also, ensure that dummy loads are connected to test set connectors J18 and J19. Damage to the equipment can result if it is operated improperly.

1. CHECK FMO WARM-UP DELAY AND ELAPSED TIME INDICATOR

a. (RT) Observe and record elapsed time indicator reading.



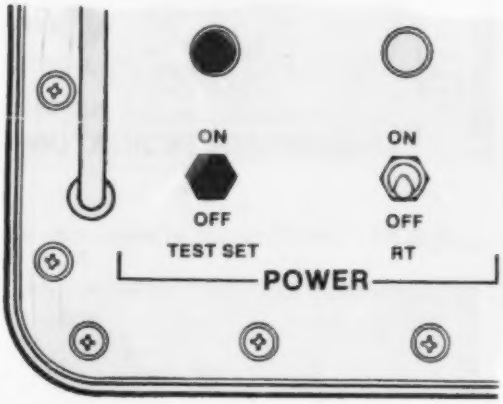
TEST PROCEDURES (Continued)

STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

b. (TS) TEST SET POWER: ON

(TS) TEST SET POWER ON indicator lights.

Check prime power source.
Refer to TM 11-6625-2883-13.


ON
OFF
TEST SET
ON
OFF
RT
POWER

c. (TS) LAMP TEST: Depress momentarily.

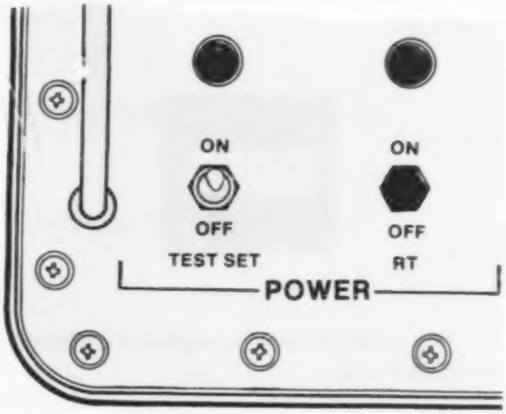
(TS) BITE FAULT, ADVISORY, and CONTROL INDICATOR section indicators light (12 indicators).

Refer to TM 11-6625-2883-13.

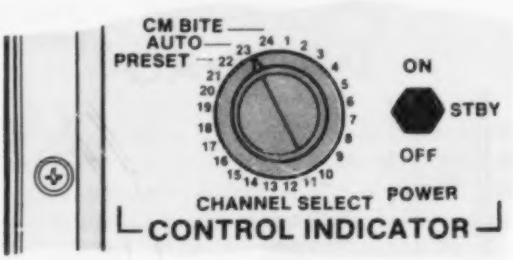
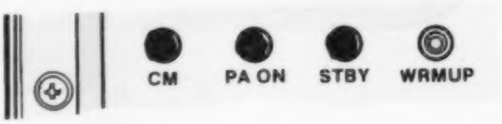
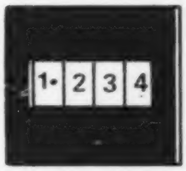
d. (TS) RT POWER: ON

(TS) RT POWER indicator lights.

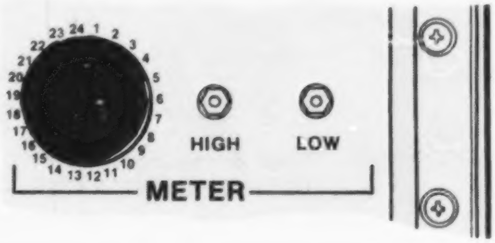
Refer to TM 11-6625-2883-13.


ON
OFF
TEST SET
ON
OFF
RT
POWER

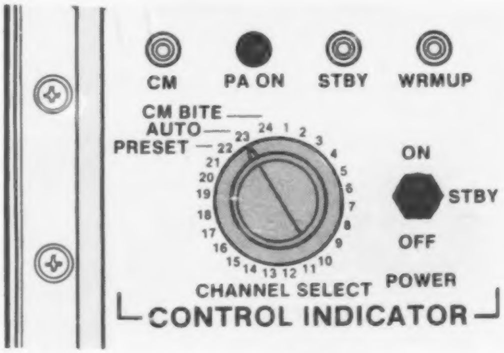
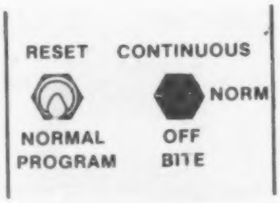
TEST PROCEDURES (Continued)

STEP	OPERATION → NORMAL INDICATION → CORRECTIVE ACTION
e.	(TS) CONTROL INDICATOR POWER: STBY (Note time)  CM BITE AUTO PRESET 24 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 ON STBY OFF CHANNEL SELECT POWER CONTROL INDICATOR (TS) RT POWER circuit breaker does not trip. Fault 1 (TS) WRMUP and STBY indicator light. Fault 2  CM PA ON STBY WRMUP (TS) BITE FAULT or ADVISORY indicators do not light or if lighted go out within 5 seconds. Fault 3 (RT) Blower operates. Replace blower. (RT) Dot located between first two most significant digits of elapsed time indicator bounces at 1 second rate. Replace ET1.  (TS) WRMUP indicator goes out within 15 seconds to 10 minutes (Note time). Replace FMO.

EST PROCEDURES (Continued)

STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
2. a.	DC VOLTAGE CHECK Observe multimeter. **NOTE** **(TS) METER switch should be in position 1.**	(Meter) Indicates +5 to +5.3 volts.	Replace PS1.
	 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 HIGH LOW METER		
b.	(TS) METER switch: 2	(Meter) Indicates +14 to +16 volts.	Replace PS1.
c.	(TS) METER switch: 3	(Meter) Indicates +22.2 to +25.8 volts.	Replace PS1.
d.	(TS) METER switch: 4	(Meter) Indicates +31 to +33 volts.	Replace PS1.
e.	(TS) METER switch: 5	(Meter) Indicates -9 to -7 volts.	Replace PS1.
f.	(TS) METER switch: 6	(Meter) Indicates -16 to -14 volts.	Replace PS1.

TEST PROCEDURES (Continued)

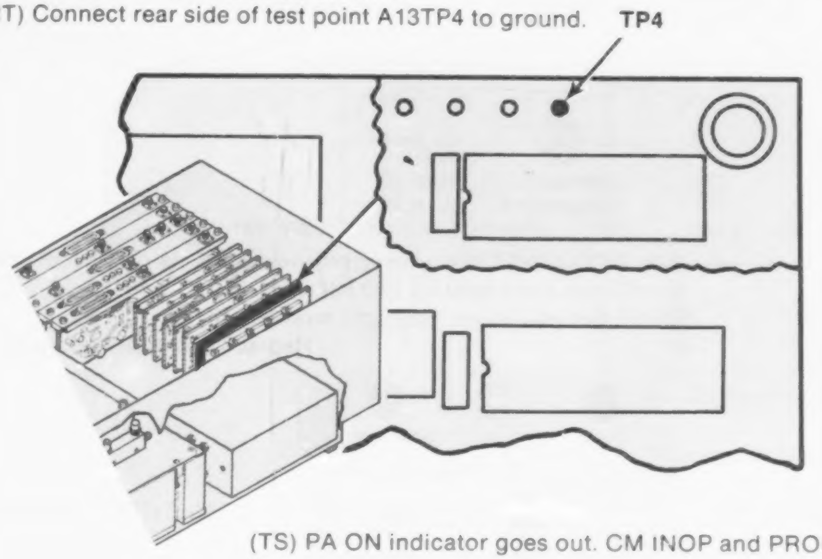
STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
g.	(TS) METER switch: 7	(Meter) Indicates -41.5 to -52.5 volts.	Replace PS1.
h.	(TS) METER switch: 16	(Meter) Indicates +14 to +16 volts.	Replace PS1.
3.	CHECK OPERATE MODE		
a.	(TS) CONTROL INDICATOR POWER: ON  CM PA ON STBY WRMUP CM BITE AUTO PRESET 24 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 ON STBY OFF CHANNEL SELECT POWER CONTROL INDICATOR	(TS) CM INOP indicator does not light.	FAULT 4
		(TS) PA ON indicator lights.	FAULTS 5, 6, 7, 8
4.	CHECK BITE		
a.	(TS) BITE: CONTINUOUS  RESET CONTINUOUS NORM NORMAL PROGRAM OFF BITE	(TS) PA ON indicator goes out. CM INOP indicator does not light.	Replace synchronizer using MAM.
b.	(TS) BITE: NORM	(TS) PA ON indicator lights.	

TEST PROCEDURES (Continued)

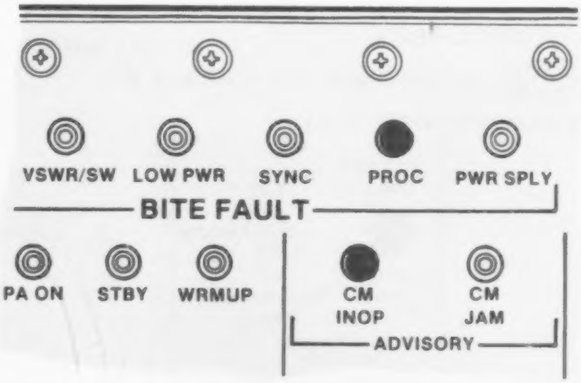
STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

5. CHECK DOPPLER PROCESSOR BITE

a. (RT) Connect rear side of test point A13TP4 to ground.



(TS) PA ON indicator goes out. CM INOP and PROC indicators light.


VSWR/SW
LOW PWR
SYNC
PROC
PWR SPLY
BITE FAULT
PA ON
STBY
WRMUP
CM INOP
CM JAM
ADVISORY

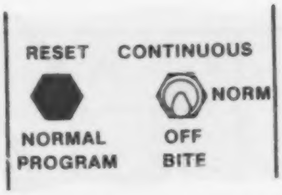
Replace doppler processor using MAM and resume testing. If fault does not clear replace synchronizer using MAM.

b. (RT) Remove ground from test point A13TP4.

(TS) CM INOP and PROC indicators go out. PA ON indicator lights.

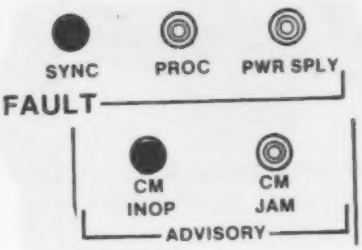
STEP | **OPERATION → NORMAL INDICATION → CORRECTIVE ACTION**

6. CHECK SYNCHRONIZER BITE
(TS) PROGRAM: RESET (momentarily)


RESET
CONTINUOUS
NORM
NORMAL PROGRAM
OFF BITE

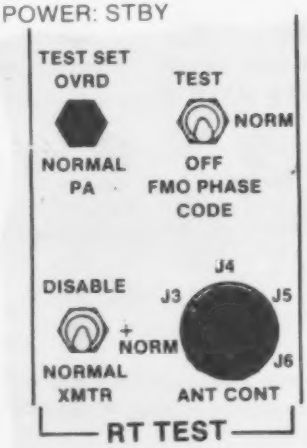
(TS) PA ON indicator goes out for two seconds. CM INOP and SYNC indicators light for two seconds. PROC and VSWR/SW indicators may light momentarily.

Replace synchronizer using MAM.


SYNC
PROC
PWR SPLY
FAULT
CM INOP
CM JAM
ADVISORY

7. CHECK DUPLEXER RF SWITCH BITE

a. (TS) PA: TEST SET OVRD
ANT CONT: J3 (Note time)
CONTROL INDICATOR POWER: STBY

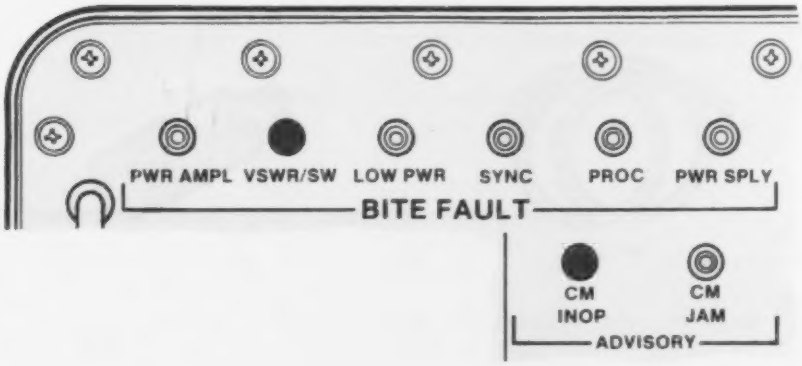

TEST SET OVRD
TEST
NORM
NORMAL PA
OFF FMO PHASE CODE
DISABLE
+ NORM
NORMAL XMTR
J3
J4
J5
J6
ANT CONT
RT TEST

(TS) PA ON indicator goes out.
STBY indicator lights.

TEST PROCEDURES (Continued)

STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

(TS) CM INOP and VSWR/SW indicators light within 30 to 90 seconds.


PWR AMPL
VSWR/SW
LOW PWR
SYNC
PROC
PWR SPLY
BITE FAULT
CM INOP
CM JAM
ADVISORY

Replace duplexer.

b. (TS) ANT CONT: J4

(TS) CM INOP and VSWR/SW indicators light within 30 to 90 seconds.

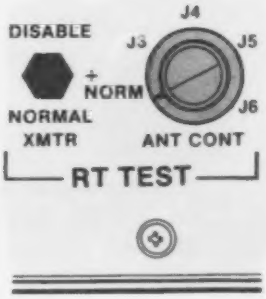
Replace duplexer.

c. (TS) ANT CONT: NORM

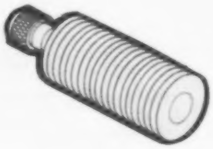
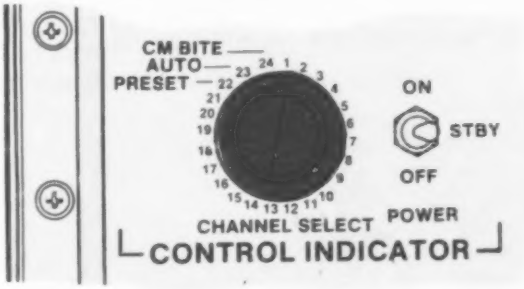
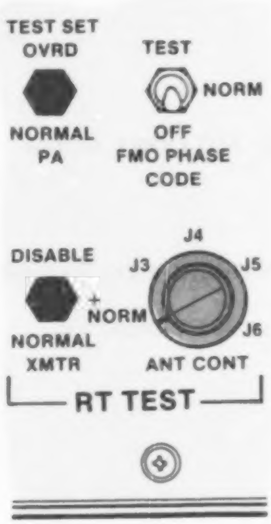
(TS) CM INOP and VSWR/SW indicators go out.

8. CHECK DUPLEXER VSWR BITE

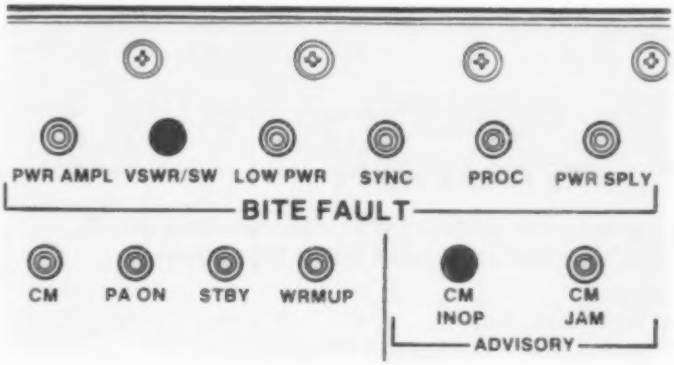
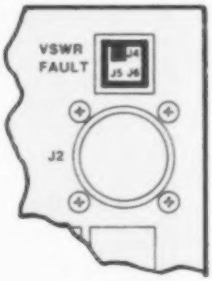
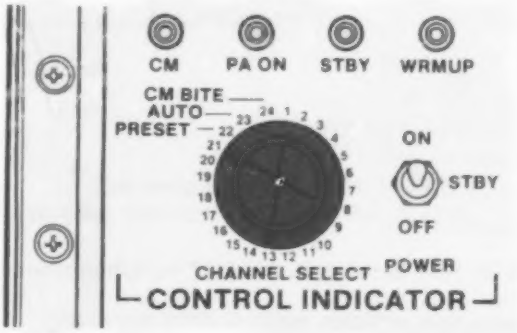
a. (TS) XMTR: DISABLE


DISABLE
+
NORM
NORMAL
XMTR
J3
J4
J5
J6
ANT CONT
RT TEST

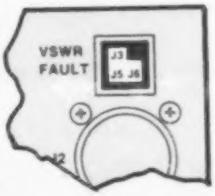
TEST PROCEDURES (Continued)

STEP	OPERATION → NORMAL INDICATION → CORRECTIVE ACTION
b.	Disconnect test cable W5 between (TS) J3 and (RT) J3.
c.	Connect attenuator AT1 (part of TS-3609) to (TS) J3.
	W10  AT1
d.	Connect special test cable W10 (part of TS-3609) to (RT) J3.
e.	(TS) CHANNEL SELECT: 1 PA: NORMAL XMTR: NORMAL
	 CM BITE AUTO PRESET 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 CHANNEL SELECT ON STBY OFF POWER CONTROL INDICATOR  TEST SET OVRD NORMAL PA TEST NORM OFF FMO PHASE CODE DISABLE NORMAL XMTR J3 J4 J5 J6 NORM ANT CONT RT TEST
	CAUTION If the following normal indications do not occur immediately, set CONTROL INDICATOR POWER switch back to STBY position.

TEST PROCEDURES (Continued)

STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
f.	(TS) CONTROL INDICATOR POWER: ON	(TS) VSWR/SW indicator lights for approximately 1/2 second. (TS) PA ON indicator goes out. CM INOP indicator lights.	Replace duplexer.
		(RT) VSWR FAULT J3 indicator lights.	Replace synchronizer.
	 PWR AMPL VSWR/SW LOW PWR SYNC PROC PWR SPLY BITE FAULT CM PA ON STBY WRMUP CM INOP CM JAM ADVISORY	 VSWR FAULT J4 J5 J6 J2	
g.	(TS) CONTROL INDICATOR POWER: STBY PROGRAM: RESET	(TS) CM INOP indicator goes out. (RT) VSWR FAULT indicator J3 goes out.	
h.	Repeat steps f and g for (TS) CHANNEL SELECT switch positions 13 and 21.		
	 CM PA ON STBY WRMUP CM BITE AUTO PRESET 24 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 ON STBY OFF POWER CHANNEL SELECT CONTROL INDICATOR		

TEST PROCEDURES (Continued)

STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
i.	(TS) CONTROL INDICATOR POWER: STBY XMTR: DISABLE		
j.	Reconnect test cable W5 between (TS) J3 and (RT) J3.		
k.	Disconnect test cable W6 between (TS) J4 and (RT) J4		
l.	Connect attenuator AT1 to (TS) J4.		
m.	Connect special test cable W10 to (RT) J4.		
n.	(TS) CHANNEL SELECT: 1 XMTR: NORMAL **CAUTION** **If the following normal indications do not occur immediately, set CONTROL INDICATOR POWER switch back to STBY position.** (TS) CONTROL INDICATOR POWER: ON	VSWR/SW indicator lights for approximately 1/2 second.	Replace duplexer.
		(TS) PA ON indicator goes out. CM INOP indicator lights. (RT) VSWR FAULT J4 indicator lights.  	Replace synchronizer.
o.	(TS) CONTROL INDICATOR POWER: STBY PROGRAM: RESET	(TS) CM INOP indicator goes out. (RT) VSWR FAULT J4 indicator goes out.	
p.	Repeat steps n and o for (TS) CHANNEL SELECT switch positions 13 and 21.		
q.	(TS) CONTROL INDICATOR POWER: OFF		
r.	Reconnect test cable W6 between (TS) J4 and (RT) J4.		

TEST PROCEDURES (Continued)

STEP	OPERATION → NORMAL INDICATION → CORRECTIVE ACTION

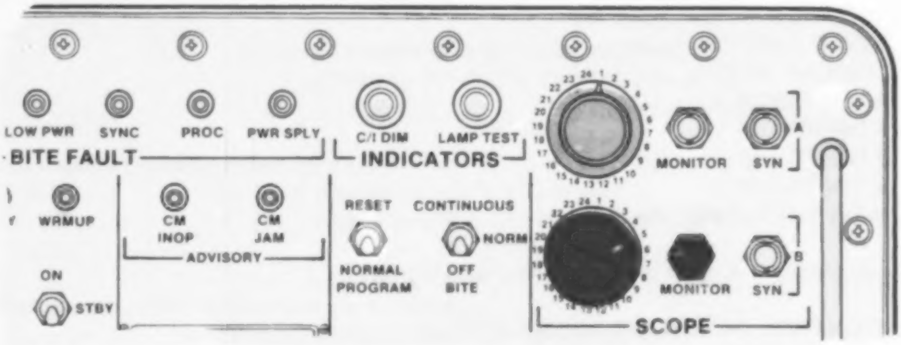
9. CHECK LOW POWER BITE FAULT CIRCUITS

a. (TS) CONTROL INDICATOR POWER: ON

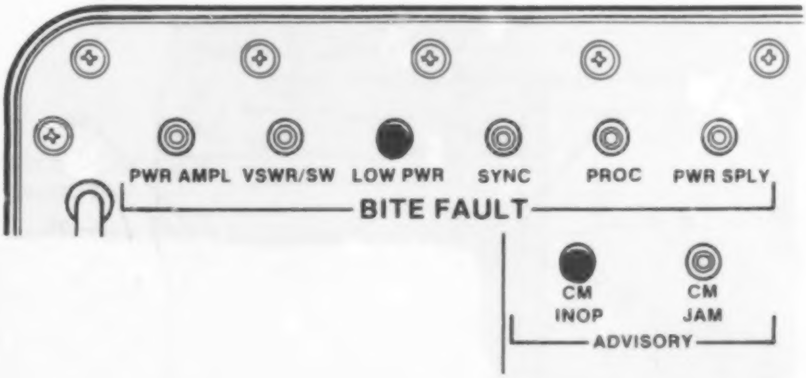
(TS) WRMUP indicator lights and goes out within 2 minutes.
(TS) PA ON indicator lights.

b. (TS) SCOPE B: 8

c. (TS) Short SCOPE B MONITOR jack to ground.


LOW PWR
SYNC
PROC
PWR SPLY
BITE FAULT
C/I DIM
LAMP TEST
INDICATORS
MONITOR
SYN
A
WRMUP
CM INOP
CM JAM
ADVISORY
RESET
CONTINUOUS
NORMAL PROGRAM
OFF BITE
NORM
ON
STBY
MONITOR
SYN
B
SCOPE

(TS) PA ON indicator goes out.
LOW PWR and CM INOP indicators light.

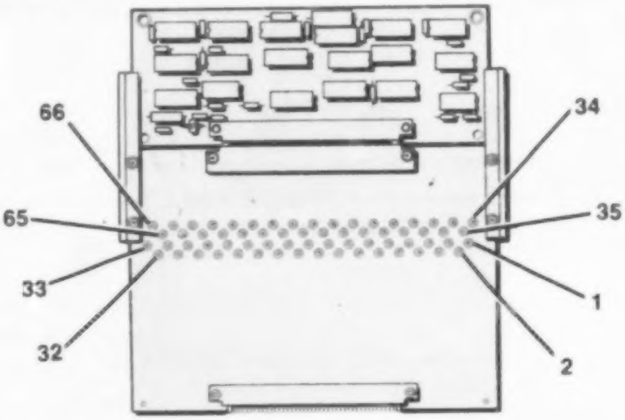

PWR AMPL
VSWR/SW
LOW PWR
SYNC
PROC
PWR SPLY
BITE FAULT
CM INOP
CM JAM
ADVISORY

Replace synchronizer.

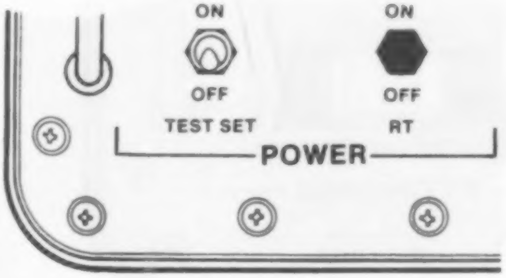
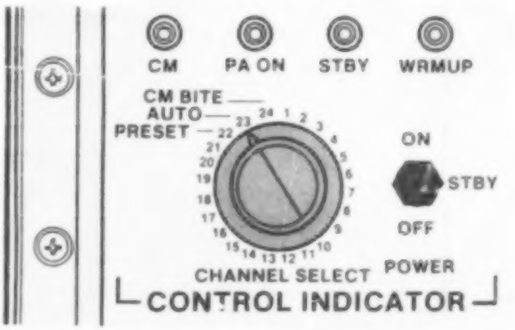
d. (TS) PROGRAM: RESET

(TS) LOW PWR and CM INOP indicators go out.
(TS) PA ON indicator lights.

TEST PROCEDURES (Continued)

STEP	OPERATION → NORMAL INDICATION → CORRECTIVE ACTION
10.	CHECK SYSTEM TIMING
a.	(Scope) Connect BNC Tee connector to channel A INPUT jack.
b.	(TS) Connect SCOPE A MONITOR jack to one end of BNC Tee connector.
c.	(Scope) Connect MAIN trigger EXT input jack to other end of BNC connector.
d.	(Scope) Set controls as follows: MAIN TRIGGER: EXT MAIN SLOPE: + MAIN ACS/ACF/AC/DC: AC MIXED TIME/CM: 1 μsec DISPLAY: ALT A VOLTS/CM: 2 A INPUT: DC B INPUT: DC B VOLTS/CM: 2 MAIN TRIG LEVEL: As required
e.	(Scope) Connect X1 test probe to channel B input.
f.	(TS) CONTROL INDICATOR POWER: OFF RT POWER: OFF
g.	(RT) Remove card assembly A7 (Para. 3-13), insert extender card into card socket, and insert card assembly into extender card. 
h.	(TS) RT POWER: ON CONTROL INDICATOR POWER: ON SCOPE A: 2 (TS) RT POWER indicator lights. WRMUP indicator lights and goes out within 2 minutes. PA ON indicator lights.

TEST PROCEDURES (Continued)

STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
i.	Connect scope probe to extender card pin 24.	(Scope) XMIT waveform is displayed (Refer to WF-1, TM 11-5865-201-30-2.)	Replace A7 card.
j.	Connect scope probe to extender card pin 27.	(Scope) R1+ waveform is displayed. (Refer to WF-2, TM 11-5865-201-30-2.)	Replace A7 card.
k.	Connect scope probe to extender card pin 25.	(Scope) R2+ waveform is displayed. (Refer to WF-3, TM 11-5865-201-30-2.)	Replace A7 card.
l.	Connect scope probe to extender card pin 40.	(Scope) R3+ waveform is displayed. (Refer to WF-4, TM 11-5865-201-30-2.)	Replace A7 card.
m.	Connect scope probe to extender card pin 61	(Scope) MBBLH waveform is displayed (Refer to WF-5, TM 11-5865-201-30-2.)	Replace A7 card.
n.	Connect scope probe to extender card pin 29.	(Scope) SYNL waveform is displayed. (Refer to WF-5, TM 11-5865-201-30-2.)	Replace A7 card.
o.	(TS) CONTROL INDICATOR POWER: OFF RT POWER: OFF  ON OFF TEST SET ON OFF RT POWER  CM PA ON STBY WRMUP CM BITE AUTO PRESET 24 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 CHANNEL SELECT ON STBY OFF POWER CONTROL INDICATOR		
p.	(RT) Remove extender card and A7 card assembly from card socket. Insert A7 card assembly into card socket.		

TEST PROCEDURES (Continued)

STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

11. CHECK RF POWER OUTPUT/FREQUENCY SELECTION

a. (TS) RT POWER: ON
(TS) CONTROL INDICATOR POWER: STBY

(TS) WRMUP indicator lights and goes out within 10 minutes.

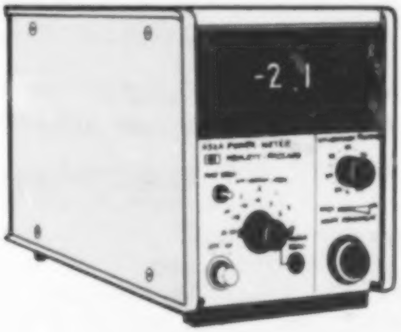
b. (Power Meter) Zero before taking readings.

c. (TS) CONTROL INDICATOR POWER: ON

(TS) PA ON indicator lights.

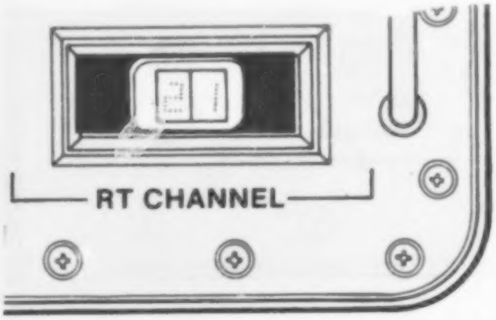
d. (TS) CHANNEL SELECT: Set to positions 1 through 21 while observing the following indication for each position.

(Power Meter) Indicates -5 to -1 dBm for all numbered positions of CHANNEL SELECT switch.



FAULTS 9, 10

(TS) RT CHANNEL indicator readout tracks CHANNEL SELECT switch positions.



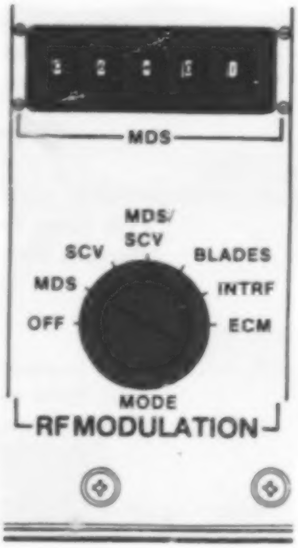
Replace synchronizer.

EST PROCEDURES (Continued)

STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

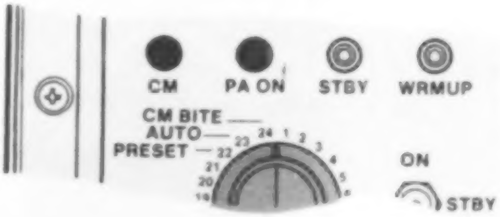
12. CHECK MDS

a. (SCOPE) SOURCE: LINE
TIME/DIV: 50 μs
VOLTS/DIV: 2


MDS
MDS/
SCV
SCV
BLADES
MDS
INTRF
OFF
ECM
MODE
RF MODULATION

b. (TS) CHANNEL SELECT: 1
SCOPE A: 6
MDS: $\boxed{0}\boxed{6}\boxed{+}\boxed{0}\boxed{1}$
RF MODULATION MODE: MDS

(TS) CM and PA ON indicators light alternately at 3 second intervals.


CM
PA ON
STBY
WRMUP
CM BITE
AUTO
PRESET
22
23
24
1
2
3
4
5
6
21
20
19
ON
STBY

(Scope) Logic low is displayed for approximately 2 seconds. Logic high is displayed for approximately 1 second.

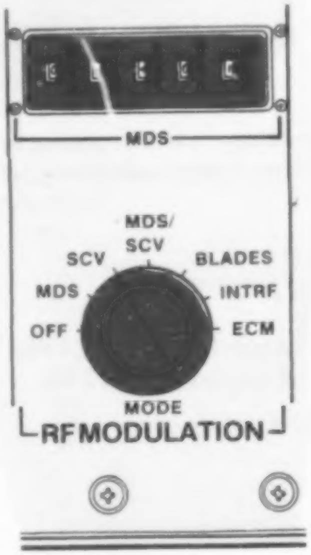
NOTE

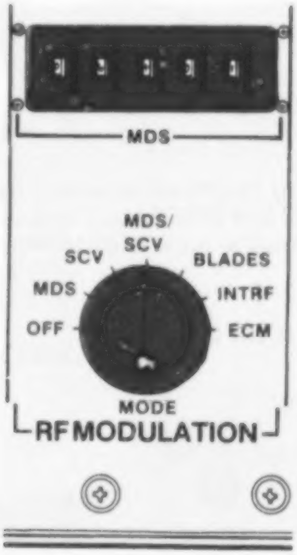
A logic high is 2.4 to 5.1 Vdc.
A logic low is 0 to 0.8 Vdc.

FAULT 11

TEST PROCEDURES (Continued)

STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
c.	(TS) CHANNEL SELECT: Repeat step a for positions 2 through 21	(TS) Same as step a. (Scope) Same as step a.	FAULT 11
d.	(TS) MDS: 11+52 CHANNEL SELECT: Set to positions 1 through 21.	(TS) Same as step a. (Scope) Same as step a.	Proceed to step e.
e.	(TS) MDS: 15+53 CHANNEL SELECT: Set to positions 1 through 21.	(TS) Same as step a. (Scope) Same as step a.	FAULT 12
13.	CHECK SCV AND FALSE ALARM RATE		
a.	(TS) MDS: 06+01 CHANNEL SELECT: 1 RF MODULATION MODE: SCV		


MDS
MDS/
SCV
SCV
BLADES
MDS
INTRF
OFF
ECM
MODE
RF MODULATION

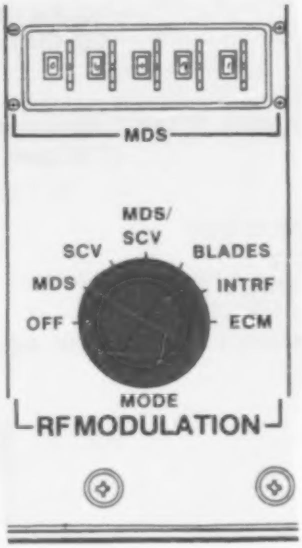
TEP	OPERATION → NORMAL INDICATION → CORRECTIVE ACTION
	(TS) PA ON indicator remains lighted. (TS) CM indicator does not light. (Observe for at least 1 minute.) Replace FMO or power supply.
b.	(TS) CHANNEL SELECT: Repeat step a for positions 2 through 21. (TS) Same as step a. Replace FMO or power supply.
4.	CHECK MDS/SCV
a.	(TS) CHANNEL SELECT: 1 MDS: 06+01 RF MODULATION MODE: MDS/SCV  MDS MDS/ SCV SCV BLADES MDS INTRF OFF ECM MODE RF MODULATION (TS) CM and PA ON indicators light at 3 second intervals. (Scope) Logic low is displayed for approximately 2 seconds, and logic high is disiplayed for approximately 1 second. Replace FMO or power supply.
b.	(TS) CHANNEL SELECT: Repeat step a for positions 2 through 21. Replace FMO or power supply.

TEST PROCEDURES (Continued)

STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

15. CHECK BLADE REJECTION

a. (TS) CHANNEL SELECT: 1
MDS: 06+71
RF MODULATION MODE. BLADES

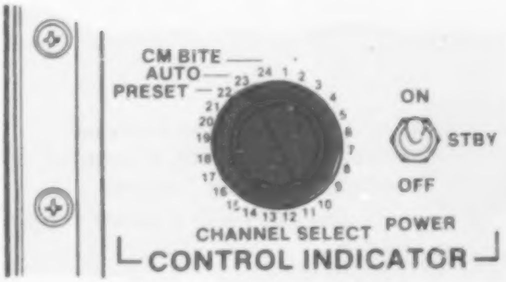

MDS
MDS/
SCV
SCV
BLADES
MDS
INTRF
OFF
ECM
MODE
RF MODULATION

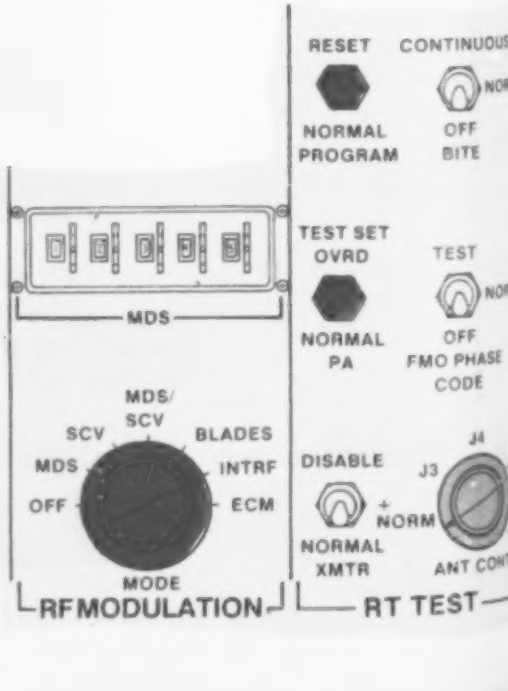
(TS) PA ON lamp remains lighted.
CM and BITE FAULT indicators do not light.
(Observe for at least 10 minutes.)

Replace doppler processor

16. CHECK INTERFERENCE MODES

a. (TS) CHANNEL SELECT: AUTO
PA: NORMAL
RF MODULATION MODE: INTRF
PROGRAM: RESET

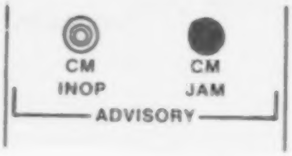

CM BITE
AUTO
PRESET
23
24
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
ON
STBY
OFF
CHANNEL SELECT
POWER
CONTROL INDICATOR


RESET
CONTINUOUS
NORMAL
PROGRAM
OFF
BITE
TEST SET
OVRD
TEST
NORMAL
PA
OFF
FMO PHASE
CODE
DISABLE
NORM
NORMAL
XMTR
J4
J3
ANT CON
RT TEST
MDS
MDS/
SCV
SCV
BLADES
MDS
INTRF
OFF
ECM
MODE
RF MODULATION

TEST PROCEDURES (Continued)

STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

(TS) PA ON indicator flashes at 10 to 20 second intervals.
(TS) CM JAM indicator lights within 30 seconds.
RT CHANNEL indicator remains on same channel.


CM
INOP
CM
JAM
ADVISORY

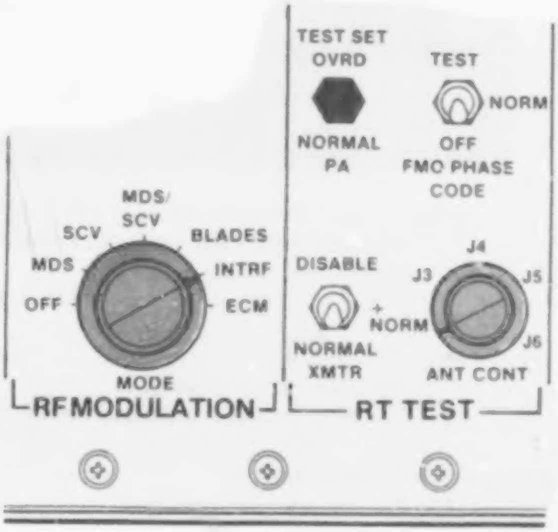
Replace first IF assembly or synchronizer.

b. (TS) RF MODULATION MODE: OFF

(TS) PA ON indicator lights.
CM JAM indicator goes out 10 seconds after PA ON indicator lights.

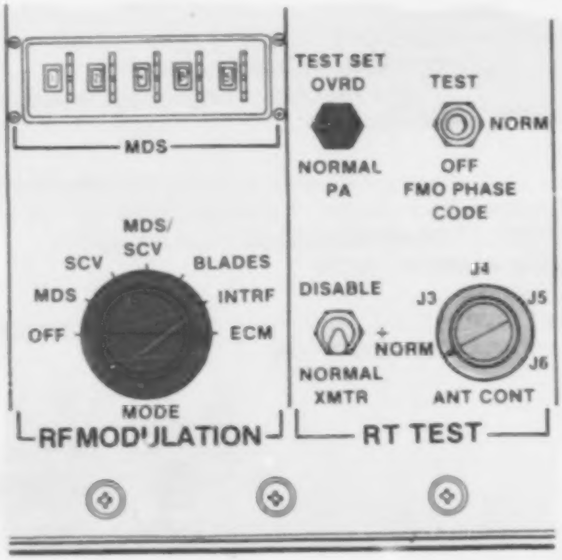
Replace synchronizer.

c. (TS) CONTROL INDICATOR POWER: STBY
RF MODULATION MODE: INTRF
ANT CONT: NORMAL
PA: TEST SET OVRD
CONTROL INDICATOR POWER: ON


TEST SET
OVRD
NORMAL
PA
TEST
NORM
OFF
FMO PHASE
CODE
MDS/
SCV
SCV
BLADES
MDS
INTRF
OFF
ECM
MODE
DISABLE
NORM
NORMAL
XMTR
J3
J4
J5
J6
ANT CONT
RF MODULATION
RT TEST

TEST PROCEDURES (Continued)

STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
		(TS) PA ON indicator lights. RT CHANNEL indication decreases from channel 13 to 1, to 21, etc. and repeats.	Replace A3 card or synchronizer.
d.	(TS) CONTROL INDICATOR POWER: STBY		
17.	CHECK ECM MODE		
a.	(TS) RF MODULATION: ECM PA: NORMAL CHANNEL SELECT: AUTO MDS: $\boxed{X}\boxed{X}\boxed{+}\boxed{8}\boxed{X}$ (X = any setting) CONTROL INDICATOR POWER: ON (Note time)		


MDS
TEST SET OVRD
NORMAL PA
TEST
NORM
OFF
FMO PHASE CODE
MDS/SCV
SCV
BLADES
MDS
INTRF
OFF
ECM
MODE
RF MODULATION
DISABLE
NORM
NORMAL XMTR
J4
J3
J5
J6
ANT CONT
RT TEST

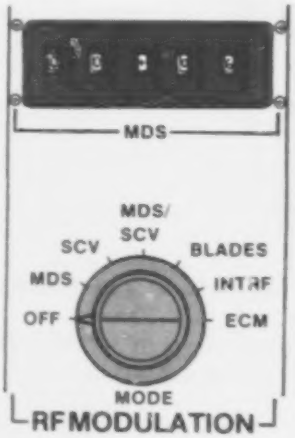
STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
		(TS) CM JAM indicator lights in about 30 seconds. RT CHANNEL indication decreases from 13 to 1, to 21 and continues.	FAULT 13
b.	(TS) RF MODULATION MODE: OFF	(TS) PA ON indicator lights. CM JAM indicator goes out within 10 seconds.	
c.	(TS) CONTROL INDICATOR POWER: STBY	(TS) PA ON indicator goes out. STBY indicator lights.	

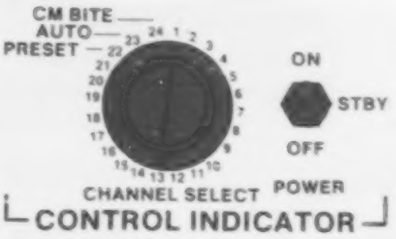
TEST PROCEDURES (Continued)

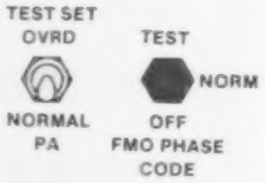
STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

18. CHECK FMO PHASE CODE

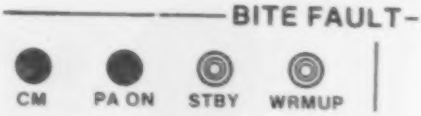
a. (TS) FMO PHASE CODE: NORM
CHANNEL SELECT: 13
MDS: 0 0 + 0 6
CONTROL INDICATOR POWER: ON


MDS
MDS/
SCV
SCV
BLADES
MDS
INTRF
OFF
ECM
MODE
RF MODULATION

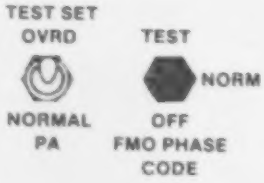

CM BITE
AUTO
PRESET
24 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
ON
STBY
OFF
CHANNEL SELECT
POWER
CONTROL INDICATOR


TEST SET
OVRD
NORMAL
PA
TEST
NORM
OFF
FMO PHASE
CODE

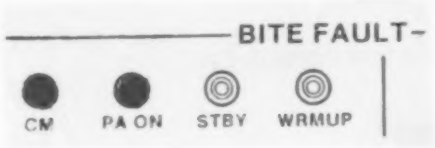
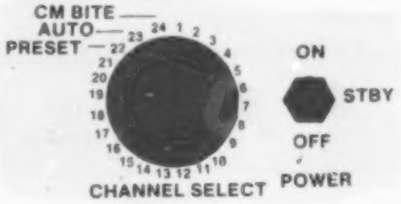
(TS) PA ON indicator lights.
CM indicator lights.


BITE FAULT-
CM
PA ON
STBY
WRMUP

b. (TS) FMO PHASE CODE: TEST
PA: TEST SET OVRD


TEST SET
OVRD
NORMAL
PA
TEST
NORM
OFF
FMO PHASE
CODE

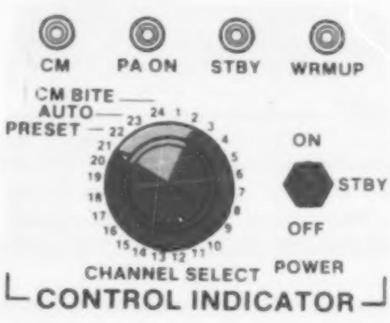
TEST PROCEDURES (Continued)

STEP	OPERATION → NORMAL INDICATION → CORRECTIVE ACTION
	(TS) PA ON indicator remains lighted. CM indicator lights FAULT 14  BITE FAULT CM PA ON STBY WRMUP
c.	(TS) FMO PHASE CODE: NORM (TS) PA ON indicator remains lighted. CM indicator goes out.
d.	(TS) MDS: 00+00
e.	CONTROL INDICATOR POWER: STBY
19.	CHECK FREQUENCY ACCURACY
a.	Disconnect test cable W13 from (TS) J17.
b.	Connect a SMA to BNC adapter to counter INPUT (DC-18 GHz) jack and connect test cable W13 to adapter.
c.	(TS) CHANNEL SELECT: 1  CM BITE AUTO PRESET 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 CHANNEL SELECT ON STBY OFF POWER
d.	(COUNTER) Set controls as follows: RESOLUTION: 100K RANGE: HI SAMPLE RATE: As required RESET: Depress momentarily (COUNTER) Indicates frequency G1 ± 1 MHz. Replace FMO.
	NOTE **Refer to TM 11-5865-201-30-2 (classified supplement) for coded frequency.**

TEST PROCEDURES (Continued)

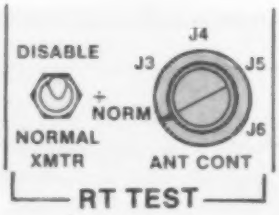
STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

e. (TS) CHANNEL SELECT: Set to positions 2 through 21 while observing counter.
(COUNTER) Indicater frequencies G2 ± 1 MHz through G21 ± 1 MHz.
Replace FMO.


CM
PA ON
STBY
WRMUP
CM BITE
AUTO
PRESET
22 23 24 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
ON
STBY
OFF
CHANNEL SELECT
POWER
CONTROL INDICATOR

20. CHECK TRANSMITTER INHIBIT MODES

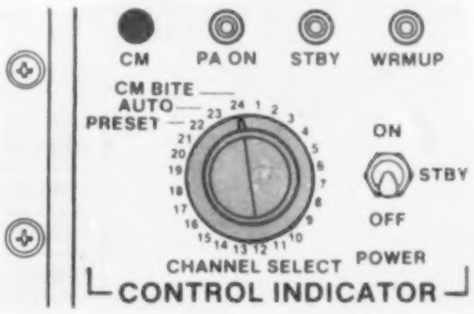
a. (TS) CONTROL INDICATOR POWER: ON
XMTR: DISABLE


DISABLE
NORMAL
XMTR
J3
J4
J5
J6
NORM
ANT CONT
RT TEST

(TS) PA ON INDICATOR goes out.
Replace synchronizer

b. (TS) XMTR: NORMAL
PROGRAM: RESET (TS) PA ON indicator lights.

c. (TS) CHANNEL SELECT: CM BITE
(TS) PA ON indicator goes out.
CM indicator flashes at 3 second intervals.


CM
PA ON
STBY
WRMUP
CM BITE
AUTO
PRESET
22 23 24 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
ON
STBY
OFF
CHANNEL SELECT
POWER
CONTROL INDICATOR

Replace synchronizer

TEST PROCEDURES (Continued)

STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
d.	(TS) CHANNEL SELECT: AUTO	(TS) PA ON indicator lights.	
21	CHECK PREHEAT MODE		
a.	(TS) CONTROL INDICATOR POWER: OFF RT POWER: OFF TEST SET POWER: OFF		
b.	Allow RT to cool for 30 minutes.		
c.	(TS) TEST SET POWER: ON	(TS) TEST SET POWER indicator lights.	
d.	Allow 10 minutes to elapse.		
e.	(TS) RT POWER: ON CONTROL INDICATOR POWER: STBY	(TS) RT POWER indicator lights. WRMUP and STBY indicator light. (TS) WRMUP indicator goes out within one minute.	Replace CM preheat assembly
22.	END OF TEST		
a.	(TS) CONTROL INDICATOR POWER: OFF RT POWER: OFF TS POWER: OFF		
b.	Disconnect test equipment and test cables.		
c.	Return test cables to storage in test set.		
d.	Replace cover on receiver transmitter.		

SECTION II.
RECEIVER TRANSMITTER TROUBLESHOOTING

SECTION CONTENTS PAGE
INTRODUCTION 3-29
MAINTENANCE ASSISTANCE MODULE 3-29
USING THE MAM 3-30
LOGIC STATES AND LEVELS 3-31
RF POWER MEASUREMENTS 3-31
TROUBLESHOOTING PROCEDURE 3-32

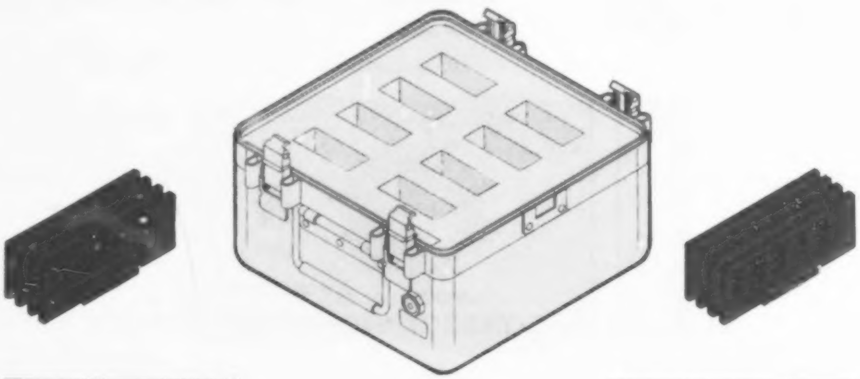
3-5. INTRODUCTION

This section contains a troubleshooting procedure which will assist you in isolating receiver transmitter faults to defective receiver transmitter assemblies. The troubleshooting chart is based upon your inability to obtain the normal indications specified in the checkout procedure given in Section 1. The fault numbers listed there correspond to those listed in the troubleshooting procedure provided here.

The troubleshooting procedures require the use of the test set to make additional checks. Therefore, you must have the receiver transmitter connected to the test set and use the standard test equipment as shown in figure 3-1 and 3-2.

3-6. MAINTENANCE ASSISTANCE MODULE

The maintenance assistance module (MAM) provided with the TS-3609/ALQ-156(V) Countermeasures Test Set is also required for fault isolation. The MAM consists of a carrying case containing the four card assemblies 1A6 through 1A9 which make up the synchronizer, and the four card assemblies 1A10 through 1A13, which make up the doppler processor. The MAM permits you to isolate a malfunction between card assemblies by the substitution method.



A6	SM-D-920686
A7	SM-D-920690
A8	SM-D-920691
A9	SM-D-920692

A10	SM-D-920693
A11	SM-D-920694
A12	SM-D-920695
A13	SM-D-920696

3-7. USING THE MAM

The CHECKS/CORRECTIVE ACTION column in the troubleshooting table will in some instances, direct you to replace the synchronizer or doppler processor card assembly groups. In this event you must use the MAM to determine by substitution which of the four cards of the set is faulty. To do this, follow this general procedure:

a. Set (TS) CONTROL INDICATOR POWER to OFF.

b. Remove one card of the four card set - either synchronizer or doppler processor - and replace it with the same card from the MAM.

c. Return to the test that you were doing when the failure occurred. Set (TS) CONTROL INDICATOR POWER switch to STBY or ON as directed in the test step and repeat the test.

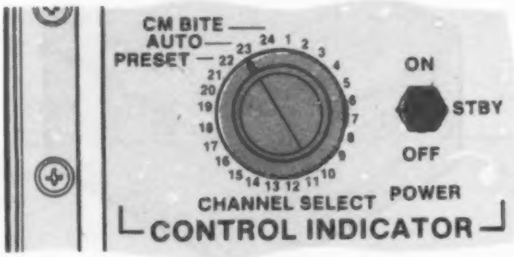
d. If you obtain the NORMAL INDICATION (failure corrected), return the MAM card assembly to its case and obtain a replacement for the failed card assembly from supply.

NOTE **Do not use the MAM card assembly as a replacement. Keep your MAM card assemblies intact.**

e. If you still do not obtain the normal indication, remove the MAM card assembly and replace it with the original card assembly that came with the RT.

f. Continue replacing card assemblies with their corresponding MAM cards and repeating the test procedure until the defective card is located.

CAUTION **Be sure to set (TS) CONTROL INDICATOR POWER to OFF when removing or replacing card assemblies. Damage to the equipment can result if cards are exchanged while power is on.**



3-8. LOGIC STATES AND LEVELS

The logic signals which you may be required to measure will be either at a high (H) or low (L) level. The mnemonic code for these signals indicates its active state. Thus, BITEH indicates that the BITE signal is active when in a high logic level. The periodic BITE check occurs when the BITE signal is high and will not occur when it is low. Similarly, the MIL signal (mutual interference low) is active when in a low state. In this state the mutual interference detection circuits are enabled.

A logic high will be from 2.4 to 5.1 volts dc while a logic low is from 0 to 0.8 volts dc.

3-9. RF POWER MEASUREMENTS

You will measure a fraction of the receiver transmitter output power as part of the RT check procedure. If troubleshooting is required, you may be directed to make other types of power measurements. Because the power meter uses a type N connector and the RF cables are type SMA or TNC, certain adaptors and an attenuator are required. A listing of these devices follows. Equivalents may be substituted.

NOTE

When making power measurements a higher negative number is less than a lower negative number, i.e., -6 dBm is less than -5 dBm.

ADAPTOR	MFG	MODEL/PART NUMBER
SMA plug to SMA jack (rt angle)	Omnispectra	219
SMA jack to N jack	Omnispectra	21010
SMA plug to N jack	Omnispectra	21030
TNC jack to SMA plug	Omnispectra	21070A
Type N, 30 dB pad	Hewlett Packard	8491A, Option 030
Type SMA, 30 dB pad	Hewlett Packard	8493A, Option 030

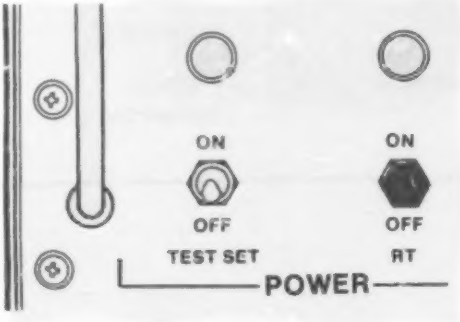
3-10. TROUBLESHOOTING PROCEDURE

The troubleshooting procedure is presented to you in tabular form. It contains three columns, as follows:

- FAULT NO.	The number in this column is keyed to the CORRECTIVE ACTION column in the test procedures given in Section I. It directs you to the applicable FAULT in the chart.
- FAULT	This column lists the fault or faults you have observed when performing the test procedure.
- CHECKS/CORRECTIVE ACTION	This column provides you with instructions for making additional checks in order to isolate a fault to a specific component. If the corrective action lists more than one assembly, replace the assemblies in the order given as they are listed in order of highest probability of failure. Repeat previous check after correcting a fault.

CAUTION

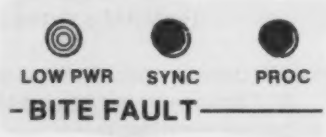
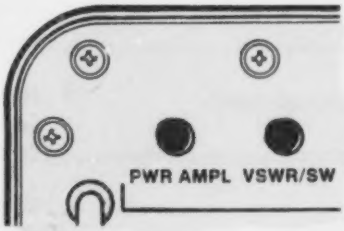
Always ensure that the CONTROL INDICATOR POWER switch is in its OFF position before inserting or removing the extender card or before disconnecting or connecting cables within the RT or between the RT and test set.

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
1.	RT POWER circuit breaker trips in standby mode. 	1. Disconnect W1P7 from power supply PS1J2 and W1P8 from PS1J3. 2. Reset RT POWER circuit breaker. If breaker does not trip, replace power supply and resume testing. 3. Reconnect W1P8 to PS1J3. If breaker trips, replace blower B1 or elapsed time indicator ET1, and resume testing.

TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
	NOTE Refer to Section III. for connector locations	4. Disconnect W1P15 from A19J1 and reset circuit breaker. If breaker does not trip, replace preheat assembly A19 and resume testing. 5. Reconnect W1P7 to PS1J2 and remove synchronizer cards A6 through A9. Reset circuit breaker. If breaker does not trip, replace synchronizer cards A6 through A9 using MAM and resume testing. 6. Replace synchronizer cards A6 through A9 and remove doppler processor cards A10 through A13. Reset circuit breaker. If breaker does not trip, replace doppler processor cards using MAM and resume testing. 7. Disconnect main harness connectors W1P3 through W1P5 and W1P10 through W1P14. Reset circuit breaker. If breaker trips, replace FMO Y1 and resume testing. 8. Reconnect W1P3 to A16J1 and reset circuit breaker. If breaker trips, replace first IF assembly and resume testing. 9. Reconnect W1P4 to A15J1 and reset circuit breaker. If breaker trips, replace duplexer and resume testing. 10. Reconnect W1P5 to AR1J1 and reset circuit breaker. If breaker trips, replace power amplifier and resume testing. 11. Reconnect W1P10 to A1J1, W1P11 to A2J1, W1P12 to A3J1, W1P13 to A4J1, and W1P14 to A5J1, one at a time, and reset circuit breaker. If breaker trips, replace applicable second IF card A1 through A5 and resume testing.

TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
2.	WRMUP indicator does not light.	Replace synchronizer cards using MAM and resume testing. If lamp still does not light,replace FMO or power supply.
	NOTE **WRMUP indicator will not light until TEST SET POWER has been on approximately 10 minutes.**	
3.	SYNC and PROC BITE FAULT indicators light. 	Extend A7 card and check for 5 MHz at pins 15 and 16. If present, replace synchronizer using MAM and resume testing. If not present, replace FMO.
	PWR AMPL BITE FAULT indicator lights.	Replace power amplifier.
		
	VSWR/SW BITE FAULT indicator lights. LOW PWR BITE FAULT	Replace duplexer and resume testing. If fault does not clear, replace synchronizer using MAM.
	CM INOP or CM INOP and SYNC indicators light.	Replace synchronizer using MAM.
	PROC BITE FAULT indicator lights.	Replace doppler processor using MAM.

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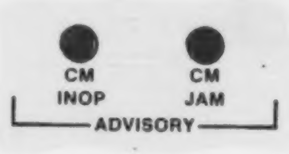
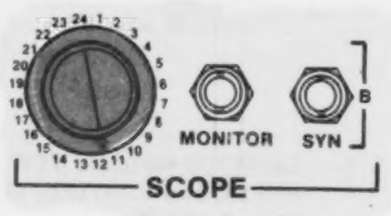
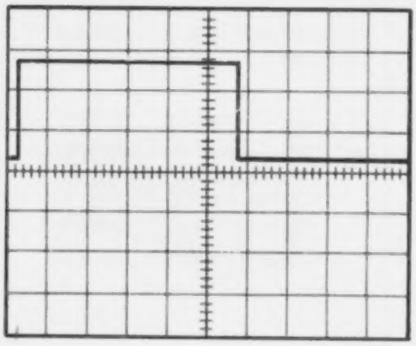
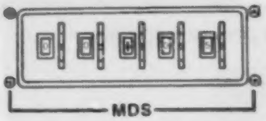
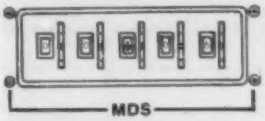
TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
3.	(Continued) PWR SPLY BITE FAULT indicator lights.	Replace power supply.
4.	 CM INOP CM JAM ADVISORY CM INOP indicator lights. BITE FAULT indicators do not light.  1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 MONITOR SYN B SCOPE Vert Sens: 2V/Div Horiz Sens: 10 msec/Div Sync: TS SYN A Center Scale: OVDC **NOTE** **Before replacing any RT assembly, first check RF connections and RF cables.**	1. Monitor SCOPE B switch positions 10, 11, and 12 for ECM waveforms shown below.  a. If waveform not present in any of the above SCOPE B switch positions, proceed to check 2. b. If waveform present in all of the above SCOPE B switch positions proceed to check 3. c. If waveform not present in 1 or 2 of the above SCOPE B switch positions, proceed to check 4.

TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
		2. Set MODE switch to MDS position and MDS switches to positions 00 + 05, 00 + 06, 00 + 07 while observing CM indicator. a. If CM indicator lights in all of the above MDS switch positions, replace duplexer first IF, or FMO. b. If CM indicator does not light in any of the above MDS switch positions, replace A8 card or STAMO.
		3. Set MODE switch to MDS position and MDS switches to positions 00 + 05, 00 + 06, and 00 + 07 while observing CM indicator. a. If CM indicator does not light in any of the above MDS switch positions, replace A8 card. b. If CM indicator does not light in MDS switch position 00 + 05, replace A2 card, or A8 card. c. If CM indicator does not light in MDS switch position 00 + 06, replace A4 card. d. If CM indicator does not light in MDS switch position 00 + 07, replace A5 card. e. If CM indicator does not light in MDS switch positions 00 + 06 and 00 + 07, replace A8 card.

TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION

4. Measure power level of 5 MHz input to second IF card realted to missing ECM waveform (see Note). Power meter should indicate 6 to 10 dBm.

NOTE

SCOPE B Position	Waveform	Second IF Card
10	ECM1L	A2
11	ECM2L	A4
12	ECM3L	A5

a. If power level is low, replace power divider or STAMO.

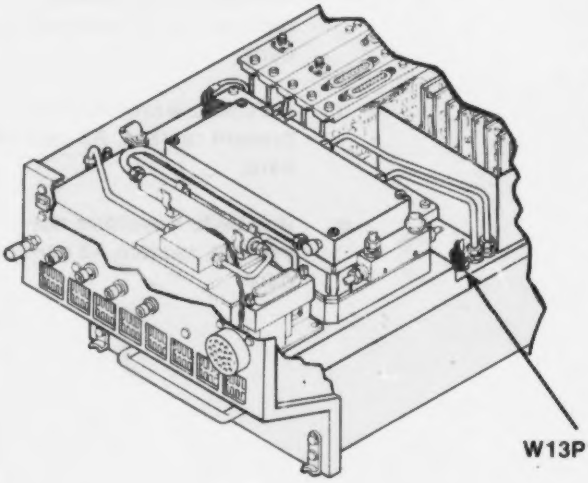
b. If ECM1L waveform not present, replace A1 card, A2 card or first IF assembly.

c. If ECM2L and ECM3L waveforms not present, replace first IF assembly or A1 card.

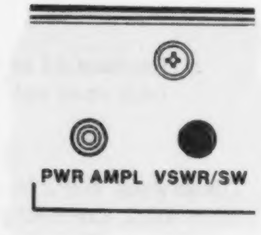
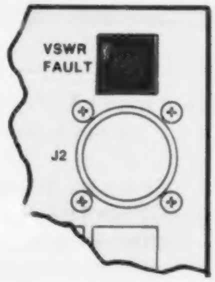
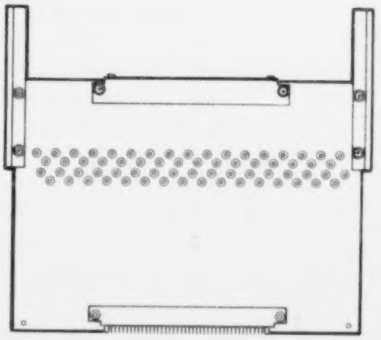
d. If ECM2L waveform not present replace, A3 card or A4 card.

e. If ECM3L waveform not present, replace A3 card or A5 card.

TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
5.	PA ON indicator does not light. **!! WARNING !!** **Set (TS) CONTROL INDICATOR POWER switch to OFF before extending cards or disconnecting cables** 	Observe power meter indication. If reading is less than -5 dBm, go to substep a. If reading is -5 dBm or greater refer to TM 11-6625-2883-13. a. Disconnect W21P1 from power amplifier AR1J3. Connect AR1J3 directly to test set J3 using cable W5 and required adaptors. Terminate test set connector J4 with 50-ohm dummy load (supplied with test set). Set (RT) BITE switch to OFF and observe power meter indication. Replace duplexer if power meter indication in greater than -5 dBm. If power meter indication is less than -5 dBm go to substep b. b. Reconnect AR1J3 to W21P1. Remove 50-ohm dummy load from test set J4. Reconnect RT to TS using cables W5 and W6 per figure 3-1. Disconnect W20P1 from AR1J2 (input). Connect power meter to W20P1 using 30 dB attenuator and required adaptors. If power meter indication is -3 dBm or greater, replace power amplifier. If power meter indication is less than -3 dBm, go to substep c.

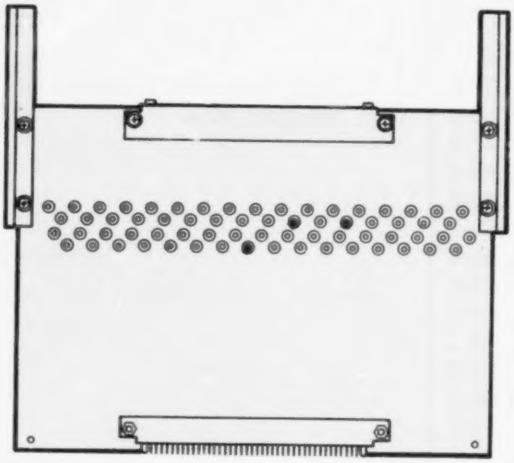
TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
5.	(Continued) **NOTE** **Refer to classified supplement for waveform WF-1.**	c. Reconnect W20P1 to AR1J2. Disconnect W12P2 from W13J1 and connect power meter to W13J1 using 30 dB attenuator and required adaptors. If power meter indication is -3 dBm or greater replace directional coupler A17. If power meter indication is less than -3 dBm, go to substep d. d. Reconnect W12P2 to W13J1. Extend A7 card and check output waveform WF-1 at pins 24 and 57. If waveform not present replace A7 card. If waveform present, replace FMO.
6.	PA ON indicator does not light. VSWR/SW indicator flashes and (RT) VSWR FAULT J3 or J4 indicator light. 	Check W5 and W6 connections between TS and RT. Replace duplexer. 
7.	PA ON indicator does not light, VSWR/SW indicator lights. **NOTE** **Refer to classified supplement for waveform WF-7.**	Extend A7 card and check output waveform WF-7 at pin 41. If waveform present, replace duplexer. If waveform not present, replace synchronizer using MAM. 

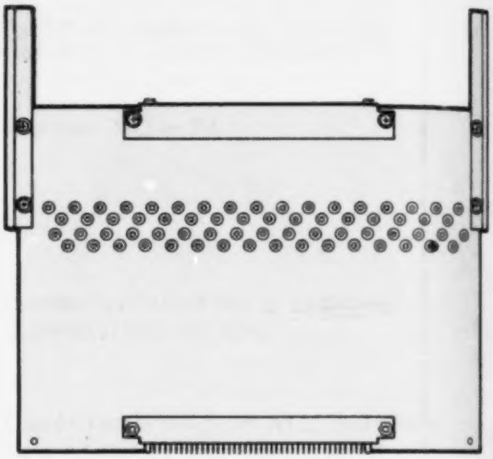
TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
8.	PA ON indicator does not light, LOW PWR indicator lights.	Proceed to FAULT NO. 5, CHECKS/CORRECTIVE ACTION
9.	Power meter indicates less than -5 dBm minimum on one or more channels, but normal in some low, midrange and high channels.	Replace FMO or PA.
10.	Power meter indicates less than -5 dBm minimum on all channels.	Proceed to FAULT No. 5, CHECKS/ CORRECTIVE ACTION.
11.	CM and PA ON indicators do not light alternately, and logic levels do not alternate.	Disconnect W8P2 from A1J2 and W9P2 from A3J2. Connect W8P2 to A3J2 and W9P2 to A1J2. Repeat step 12 a and b of test procedure. a. Replace first IF assembly A16 if fault clears. b. Replace A1 or A2 card assemblies if fault does not clear.
12.	CM and PA ON indicators do not light alternately and logic levels do not alternate when performing steps 12c or d of test procedure (note which step).	Disconnect W8P2 from A1J2 and W9P2 from A3J2. Connect W8P2 to A3J2 and W9P2 to A1J2. Repeat steps 12 a and b of test procedure. a. Replace first IF assembly A16 if fault clears. b. Replace A3 card assembly if fault remains for both steps c and d. c. Replace A4 card assembly if fault remains for step c only. d. Replace A5 card assembly if fault remains for step d only.

TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
13.	CM JAM indicator does not light, and RT CHANNEL indication does not change.	Extend A7 card and observe ECM waveforms at extender pins 47, 43 and 18 with (TS) BITE switch set to CONTINUOUS. (Refer to Fault No. 4.)  a. Replace second IF A2 card if waveform not present at pin 47. b. Replace second IF A4 card assembly if waveform not present at pin 43. c. Replace second IF A5 card if waveform not present at pin 18. d. Replace duplexer if waveform not present at all pins. Replace synchronizer using MAM if fault does not clear.
	PA ON and CM indicators do not light	
14.	CM indicator does not light.	Extend A8 card and observe waveform WF-8 at extender pin 4.

TROUBLESHOOTING PROCEDURE (Continued)

FAULT NO.	FAULT	CHECKS/CORRECTIVE ACTION
14.	(Continued) **NOTE** **Refer to classified supplement for waveform WF-8.**	 a. Replace synchronizer using MAM if waveform not present. b. Replace FMO if waveform present.

SECTION III.
RECEIVER TRANSMITTER DISASSEMBLY AND ASSEMBLY

SECTION CONTENTS **PAGE**

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3-11. GENERAL

The replacement procedures contained in this section will enable you to replace any subassembly of the receiver transmitter. The Maintenance Authorization Chart (MAC) contained in Appendix B of TM 11-5865-201-12 lists these items as replaceable at your maintenance level (AVIM). You may wish to refer to the Section II of Chapter 1, Equipment Description and Data and to figure FO-1, the receiver transmitter cabling diagram as aids in identifying subassemblies and the electrical cables connected to them.

The cover of the receiver transmitter must be removed first before you can remove any subassembly.

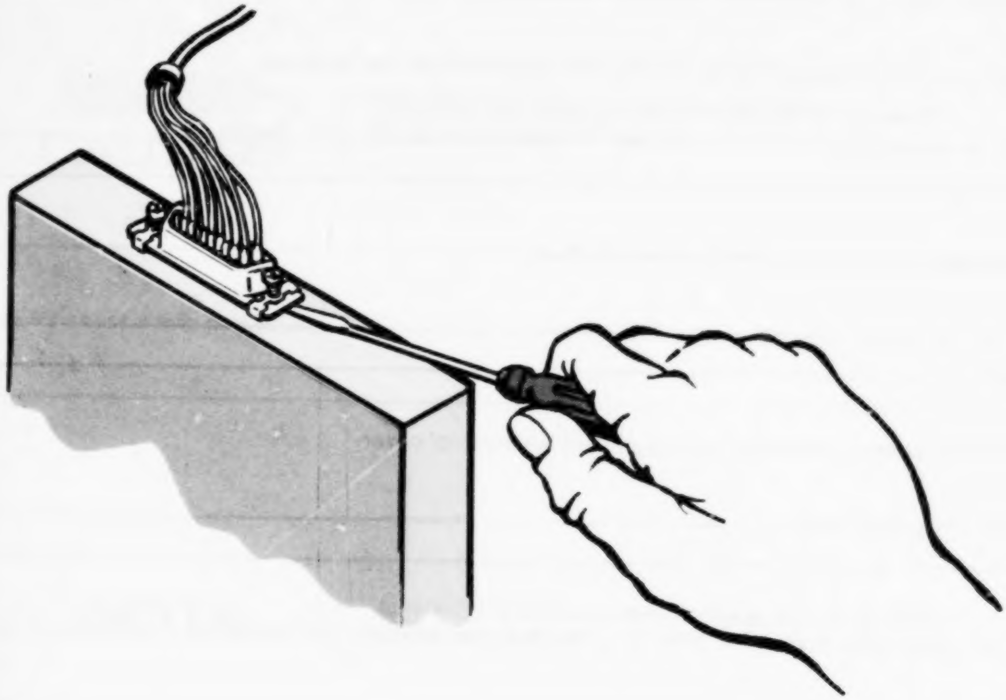
After replacement of a subassembly, you must perform the receiver transmitter check procedure given in Section I of this chapter.

When disconnecting hardline cable connectors, it is advisable to loosen the connector on the opposite end of the cable so that you can push the disconnected cable connector away from the subassembly to be replaced.

CAUTION

Never bend or deform hardline cables. Only minor flexing of these cables is permitted.

When disconnecting multipin connectors attached to the wiring harness, it is helpful to separate the connectors by use of a small screwdriver placed under the connector flange.



CAUTION

Do not attempt to disconnect wiring harness connector by pulling on the harness. Wires could be pulled loose from the connector.

The clips which hold the screws used to hold mating multipin connectors together may sometime come loose from the connector flange. After placing clip back on flange it is advisable to squeeze them together to prevent them from falling off again.

3-12. REPLACEMENT OF COVER

REMOVAL

1

Remove four machine screws and four flat washers from rear of cover.

2

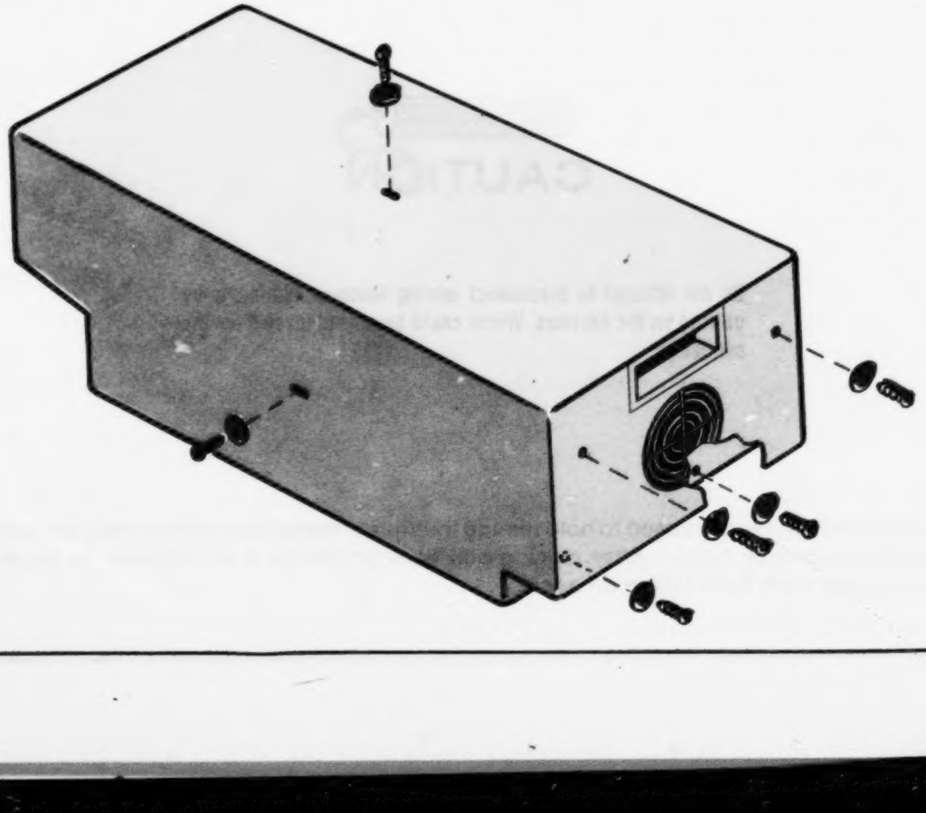
Remove screw and washer from top of cover.

3

Remove screw and washer from right and left sides of cover.

4

Pull cover away from RT chassis by grasping sides of cover and handle on front panel of RT



3-12. REPLACEMENT OF COVER (Continued)

REPLACEMENT

CAUTION

Ensure that front edges of cover slide into channel on front of chassis and compress RT gasket.

1

Slide RT chassis into cover.

NOTE

Ensure that cables do not catch on edge of cover as chassis is pushed into cover.

2

Insert four screws and flat washers into rear of cover. Tighten screws.

3

Replace screw and washer on left and right sides of cover.

4

Replace screw and washer on top of cover.

3-13. REPLACEMENT OF SYNCHRONIZER AND SIGNAL PROCESSOR ASSEMBLIES

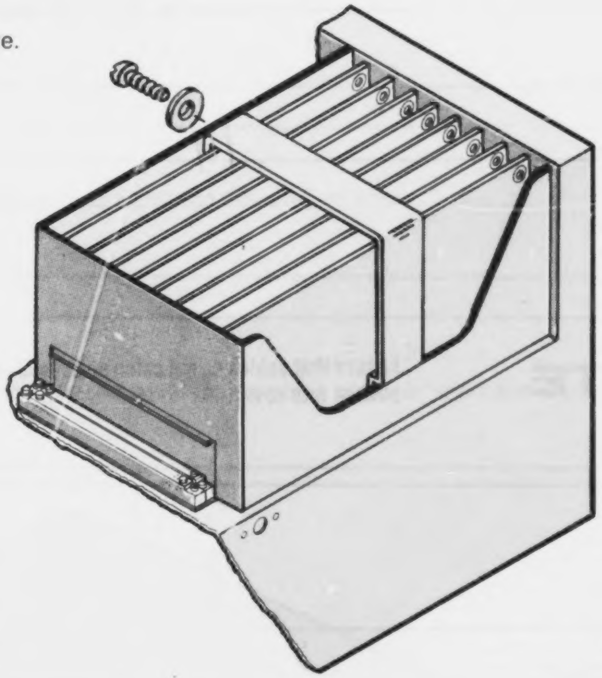
REMOVAL

1

Loosen but do not remove screw and flat washer securing strap to center card cage.

2

Raise strap and remove.



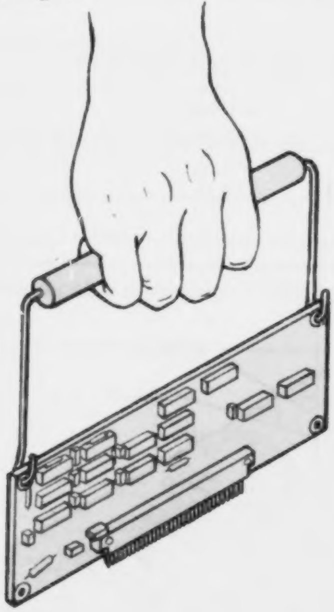
NOTE

The other end (curved end) of the strap inserts in a slot in the right side of card cage.

3-13. REPLACEMENT OF SYNCHRONIZER AND SIGNAL PROCESSOR ASSEMBLIES (Continued)

REMOVAL (Continued)

3 Insert card extractor (part of test set) into holes on circuit card assembly and pull card gently out of card cage.



NOTE

The synchronizer consists of circuit cards A6 through A9, and the signal processor consists of circuit cards A10 through A13. If the check or troubleshooting procedures direct you to replace the synchronizer or signal processor, use the MAM to locate the defective card in the set.

REPLACEMENT

1 Install replacement card by inserting it into slot guides and pressing down gently until card is firmly seated.

NOTE

Be sure and insert correct card in its own card slot. Card connectors are keyed so that a card cannot be fully inserted into wrong slot.

NOTE

If pins have been bent, card cannot be inserted. Straighten bent pins carefully using a needle-nose pliers.

2 Replace strap and tighten screw on center edge of card cage.

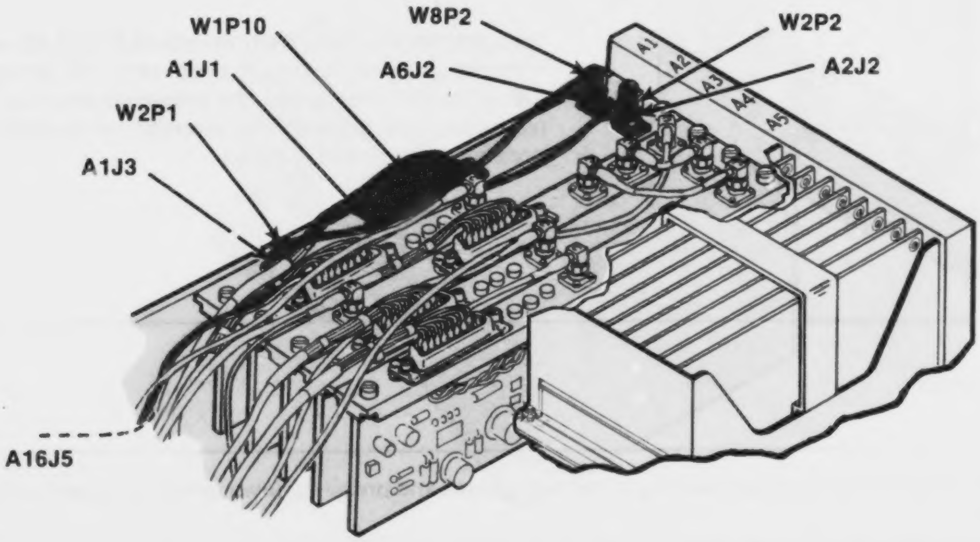
3-14. REPLACEMENT OF SECOND IF A1 CARD ASSEMBLY

REMOVAL

1

Disconnect the following cable connections:

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W8P1	A16J5
W8P2	A1J2
W2P1	A1J3
W2P2	A2J2


W1P10
W8P2
W2P2
A1J1
A6J2
A2J2
W2P1
A1J3
A16J5
A1
A2
A3
A4
A5

2

Loosen two screws securing harness connector W1P10 to A1J1. Disconnect connectors.

3

Loosen the two captive screws securing card assembly to chassis.

4

Remove card assembly by pulling up on captive screws.

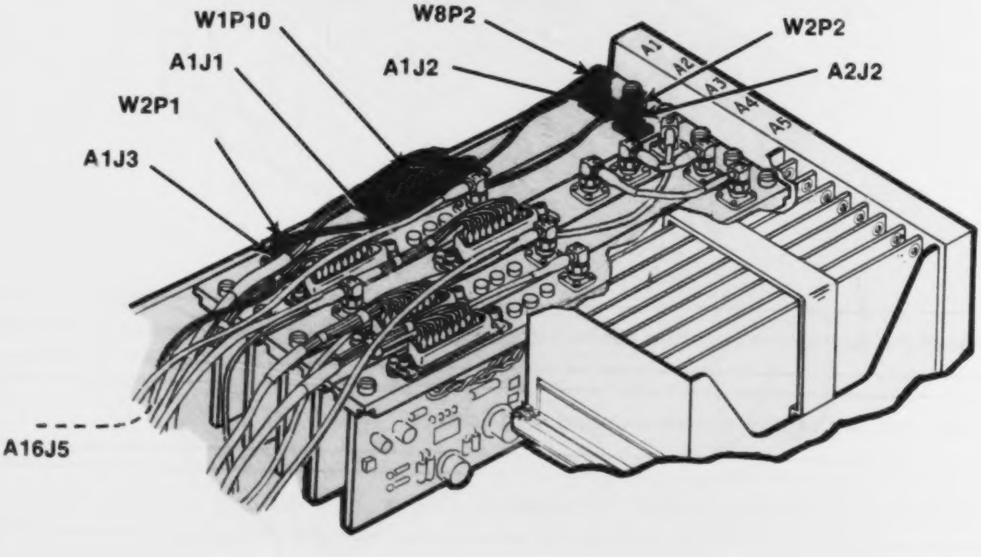
3-14. REPLACEMENT OF SECOND IF A1 CARD ASSEMBLY (Continued)

REPLACEMENT

1 Insert card assembly into card slot.

2 Tighten the two captive screws to secure card assembly to chassis.

3 Connect cable connector W1P10 to A1J1 and tighten connector screws.


W1P10
W8P2
W2P2
A1J1
A1J2
A2J2
W2P1
A1J3
A16J5
A1
A2
A3
A4
A5

4 Make the following cable connections and torque to 8-in. lbs.

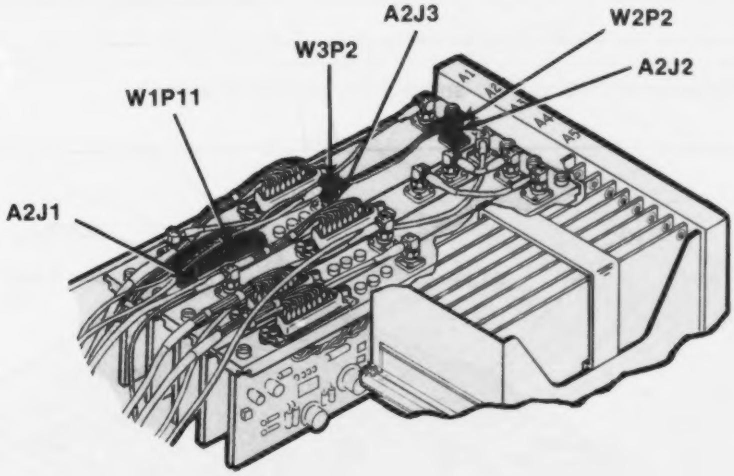
CABLE CONNECTOR	ASSEMBLY CONNECTOR
W2P2	A2J2
W2P1	A1J3
W8P2	A1J2
W8P1	A16J5

3-15. REPLACEMENT OF SECOND IF A2 CARD ASSEMBLY

REMOVAL

1 Disconnect the following cable connections:

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W2P2	A2J2
W3P2	A2J3



2 Loosen the two screws securing harness connector W1P11 to A2J1. Disconnect connectors.

3 Loosen the two captive screws securing card assembly to chassis.

4 Remove card assembly by pulling up on captive screws.

NOTE

Push cabling to one side when removing card assembly.

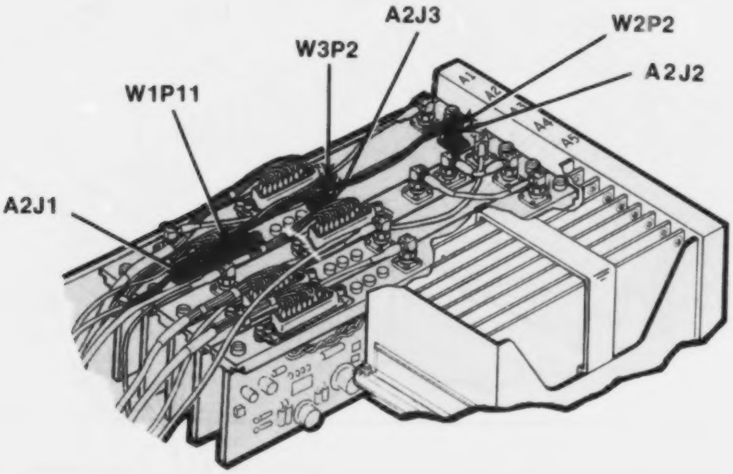
3-15. REPLACEMENT OF SECOND IF A2 CARD ASSEMBLY (Continued)

REPLACEMENT

1 Insert card assembly into card slot.

2 Tighten the two captive screws to secure card assembly to chassis.

3 Connect cable connector W1P11 to A2J1 and tighten connector screws.



4 Make the following cable connections and torque to 8 in.-lbs.

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W3P1	A2J3
W2P2	A2J2

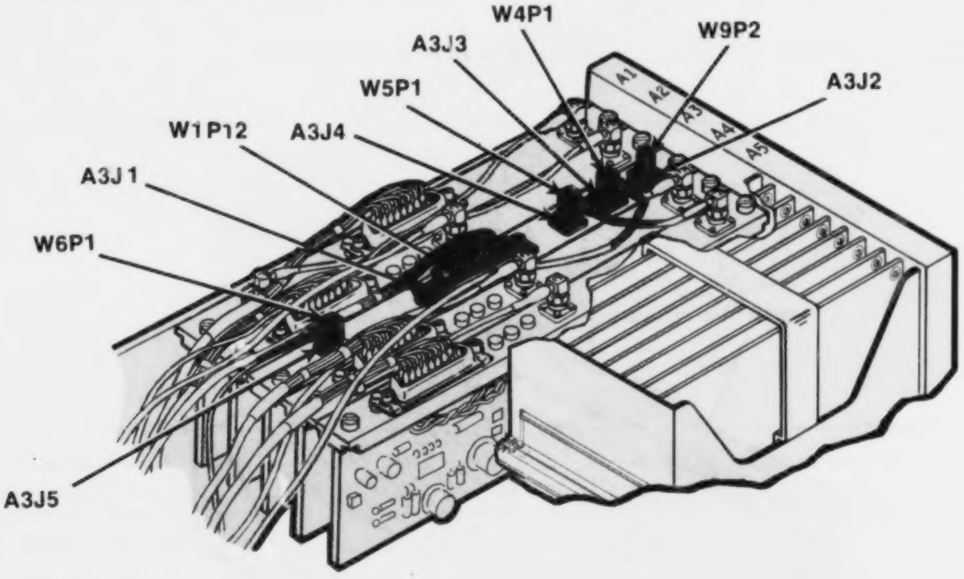
3-16. REPLACEMENT OF SECOND IF A3 CARD ASSEMBLY

REMOVAL

1

Disconnect the following cable connections:

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W4P1	A3J3
W5P1	A3J4
W6P1	A3J5
W9P2	A3J2


W4P1
A3J3
W9P2
A3J2
W5P1
W1P12
A3J4
A3J1
W6P1
A3J5
A1
A2
A3
A4
A5

2

Loosen the two screws securing harness connector W1P12 to A3J1. Disconnect connectors.

3

Loosen the two captive screws securing card assembly to chassis.

4

Remove card assembly by pulling up on captive screws.

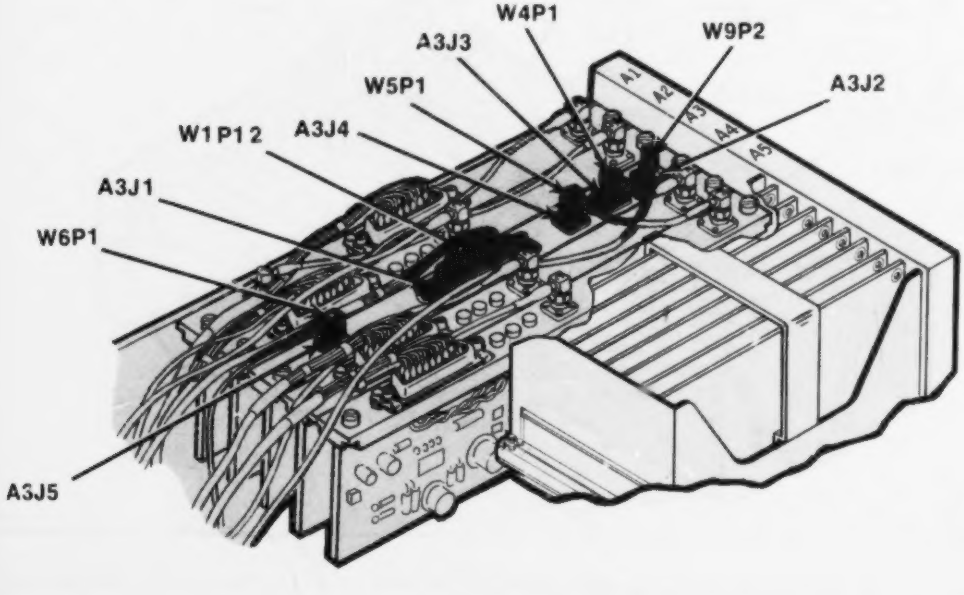
3-16. REPLACEMENT OF SECOND IF A3 CARD ASSEMBLY (Continued)

REPLACEMENT

1 Insert card assembly into card slot.

2 Tighten the two captive screws to secure card assembly to chassis.

3 Connect cable connector W1P12 to A3J1 and tighten connector screws.


W4P1
A3J3
W9P2
W5P1
A3J2
W1P12
A3J4
A3J1
W6P1
A3J5
A1
A2
A3
A4
A5

4 Make the following cable connections and torque to 8-in. lbs.

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W4P1	A3J3
W5P1	A3J4
W6P1	A3J5
W9P2	A3J2

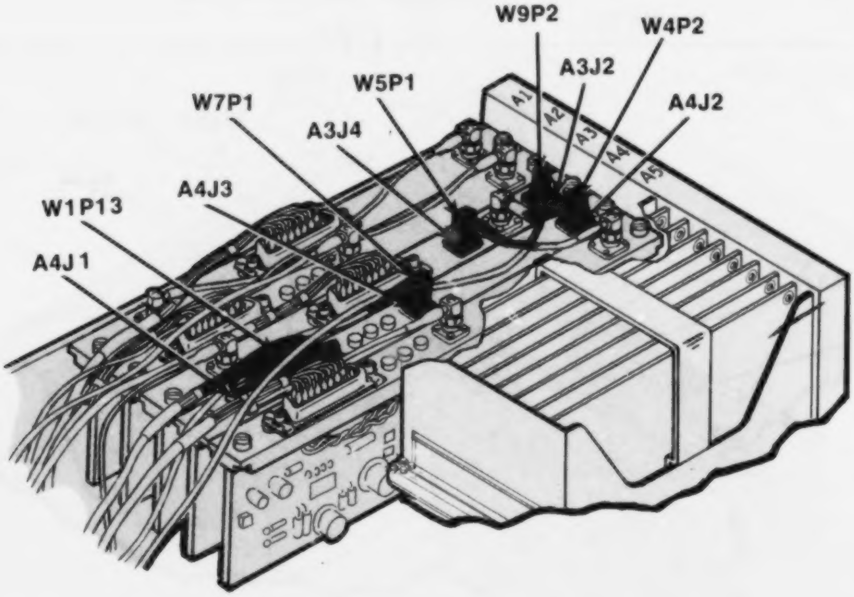
3-17. REPLACEMENT OF SECOND IF A4 CARD ASSEMBLY

REMOVAL

1

Disconnect the following cable connections:

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W5P1	A3J4
W9P2	A3J2
W4P2	A4J2
W7P1	A4J3


W9P2
W4P2
A3J2
W5P1
W7P1
A4J2
A3J4
A4J3
W1P13
A4J1
A1
A2
A3
A4
A5

2

Loosen the two screws securing harness connector W1P13 to A4J1. Disconnect connectors.

3

Loosen the two captive screws securing card assembly to chassis.

4

Remove card assembly by pulling up on captive screws

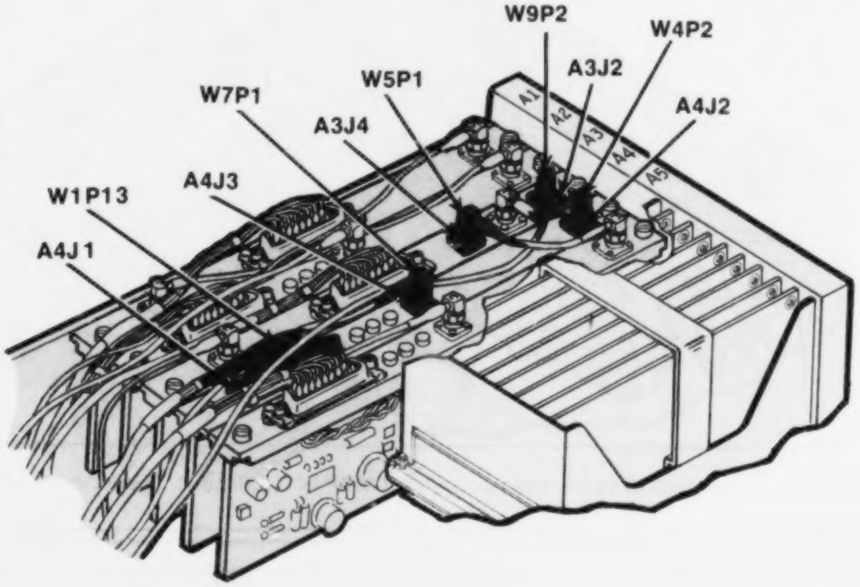
3-17. REPLACEMENT OF SECOND IF A4 CARD ASSEMBLY (Continued)

REPLACEMENT

1 Insert card assembly into card slot.

2 Tighten the two captive screws to secure card assembly to chassis.

3 Connect cable connector W1P13 to A4J1 and tighten connector screws.


W9P2
W4P2
A3J2
W5P1
W7P1
A4J2
A3J4
A1
A2
A3
A4
A5
W1P13
A4J3
A4J1

4 Make the following cable connections and torque to 8 in.-lbs.

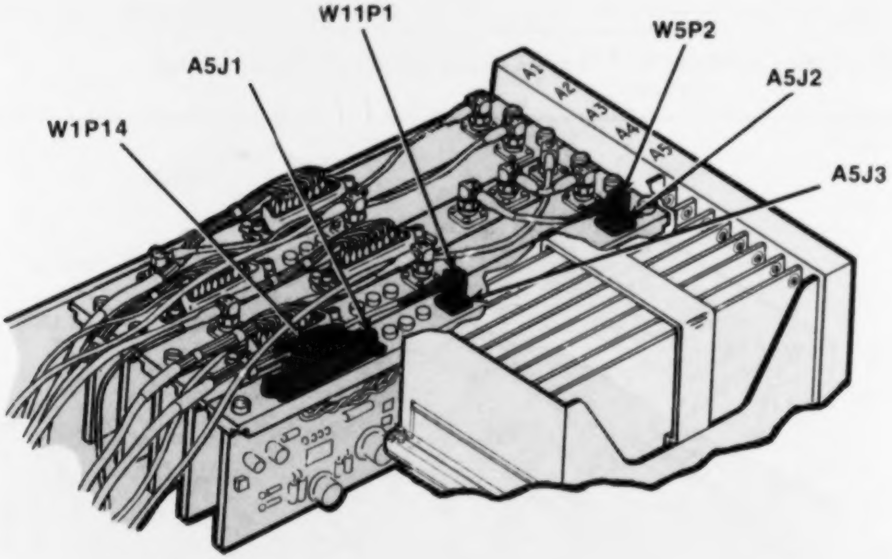
CABLE CONNECTOR	ASSEMBLY CONNECTOR
W7P1	A4J3
W4P2	A4J2
W9P2	A3J2
W5P1	A3J4

3-18. REPLACEMENT OF SECOND IF A5 CARD ASSEMBLY

REMOVAL

1 Disconnect the following cable connections:

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W5P2	A5J2
W11P1	A5J3



2 Loosen the two screws securing harness connector W1P14 from A5J1. Disconnect connectors.

3 Loosen the two captive screws securing card assembly to chassis.

4 Loosen screw and flat washer securing strap to center edge of synchronizer and signal processor card cage. Remove strap.

5 Remove card assembly by pulling up on captive screws.

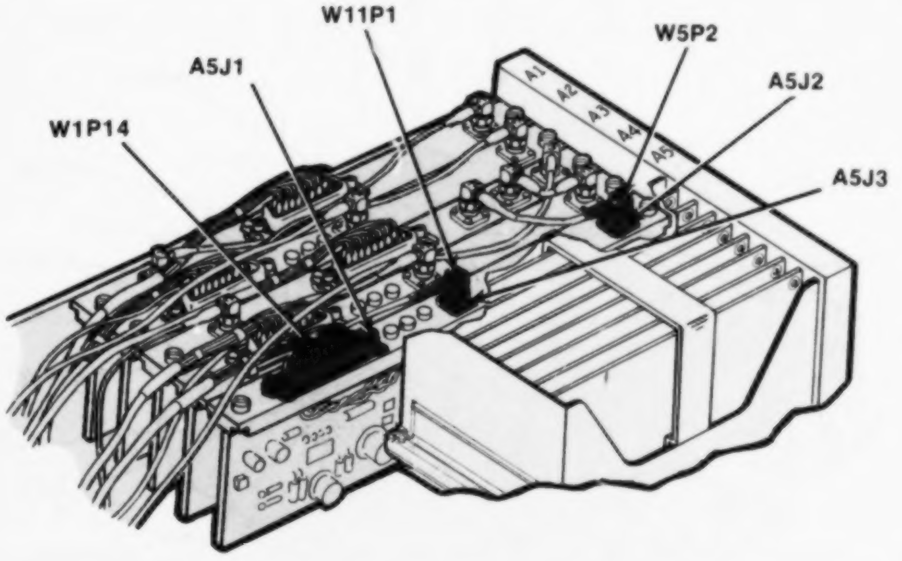
3-18. REPLACEMENT OF SECOND IF A5 CARD ASSEMBLY (Continued)

REPLACEMENT

1 Insert card assembly into card slot.

2 Tighten the two captive screws to secure card assembly to chassis.

3 Connect cable connector W1P14 to A5J1 and tighten connector screws.



4 Make the following cable connections and torque to 8 in.-lbs.

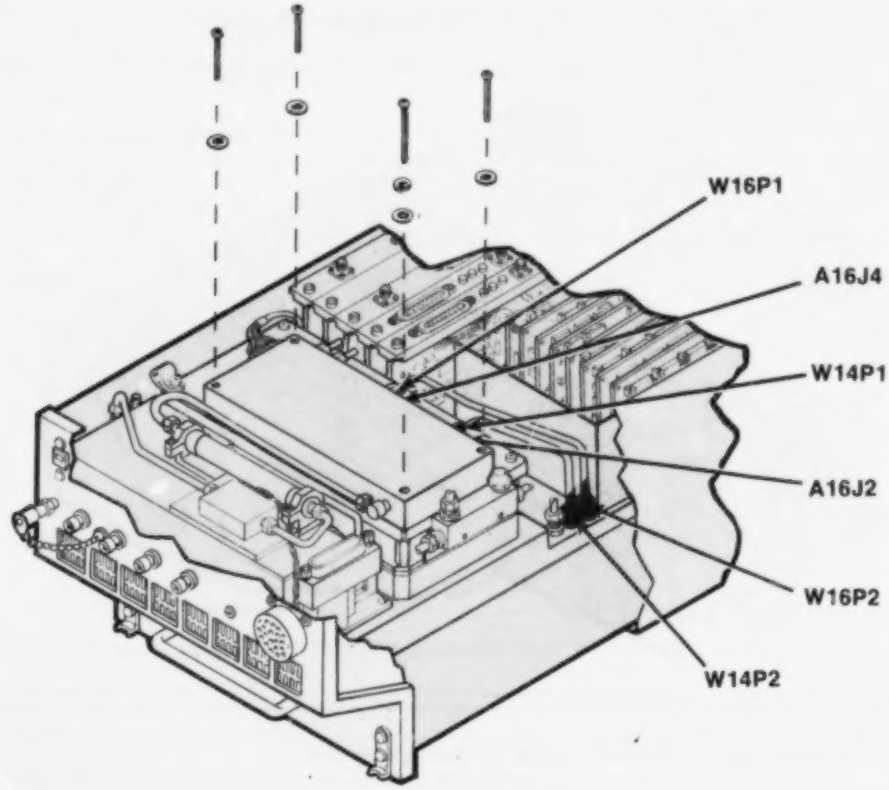
CABLE CONNECTOR	ASSEMBLY CONNECTOR
W11P1	A5J3
W5P2	A5J2

5 Replace strap and tighten screw on center edge of card synchronizer and signal processor card cage.

3-19. REPLACEMENT OF FIRST IF ASSEMBLY A16

REMOVAL

1 Loosen hard-line connectors W14P2 and W16P2.


W16P1
A16J4
W14P1
A16J2
W16P2
W14P2

2 Disconnect W14P1 from A16J2 and W16P1 from A16J4.

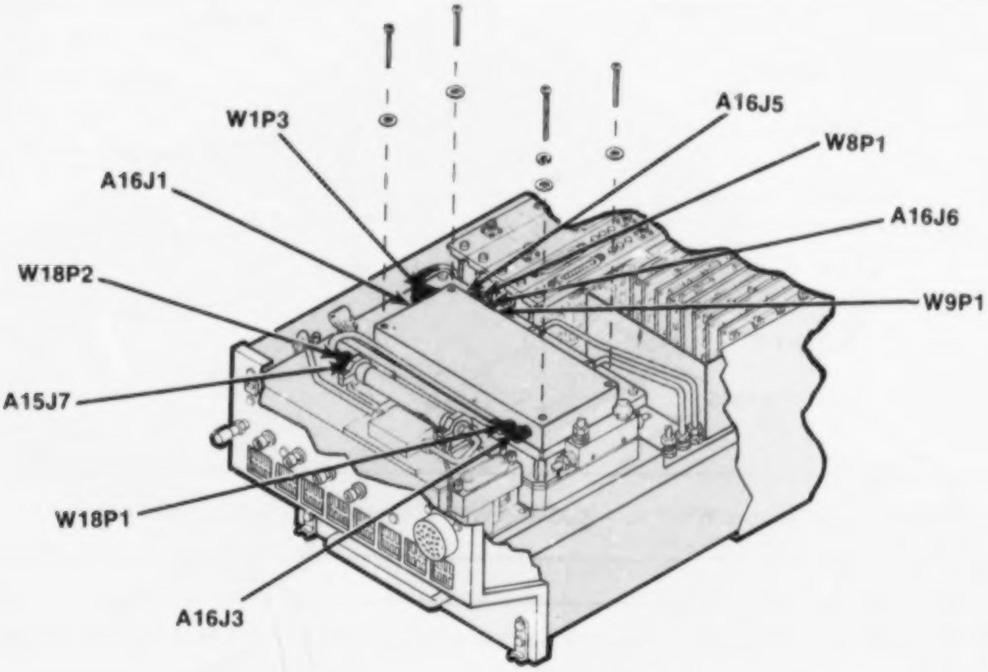
3-19. REPLACEMENT OF FIRST IF ASSEMBLY A16 (Continued)

REMOVAL (Continued)

3 Disconnect W18P1 from A16J3 and W18P2 from A15J7. Remove W18.

4 Disconnect W8P1 from A16J5 and W9P1 from A16J6.

5 Loosen two screws securing harness connector W1P3 to A16J1. Disconnect connectors.


W1P3
A16J5
W8P1
A16J1
A16J6
W18P2
W9P1
A15J7
W18P1
A16J3

6 Remove three screws and three flat washers from first IF assembly.

7 Remove one screw, one lockwasher and one flat washer from front right corner of first IF assembly. Remove assembly.

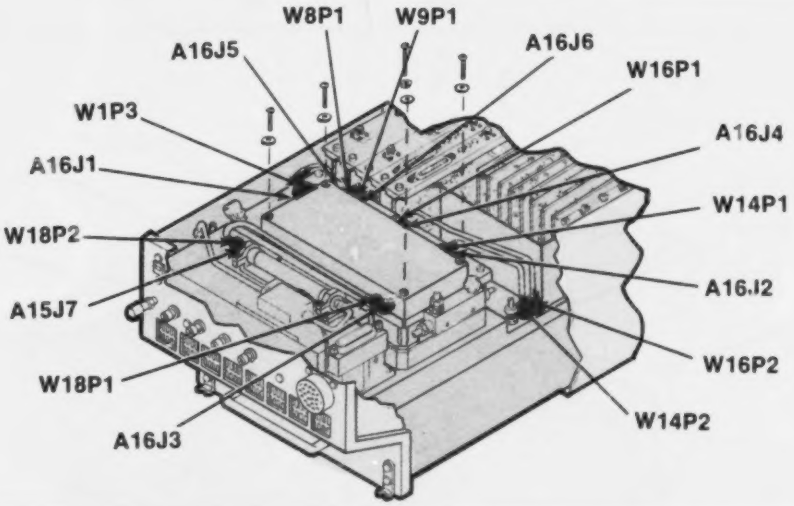
3-19. REPLACEMENT OF FIRST IF ASSEMBLY A16 (Continued)

REPLACEMENT

1 Place first IF assembly in position on top of mounting plate.

2 Replace 1-1/2 in. screw, lockwasher and flat washer attaching front right corner of first IF assembly to mounting plate. Replace remaining three 1-1/4 in. screws and flat washers.

3 Connect cable connector W1P3 to A16J1 and tighten connector screws.


W8P1
W9P1
A16J5
A16J6
W16P1
W1P3
A16J4
A16J1
W14P1
W18P2
A16J2
A15J7
W16P2
W18P1
W14P2
A16J3

4 Connect cable connectors W8P1 to A16J5 and W9P1 to A16J6. Torque connectors to 8 in. - lbs.

5 Place cable W18 in position and connect W18P1 to A16J3 and W18P2 to A15J7. Torque connectors to 8 in.-lbs.

6 Connect cable connectors W14P1 to A16J2 and W16P1 to A16J4. Torque connectors to 8 in.-lbs.

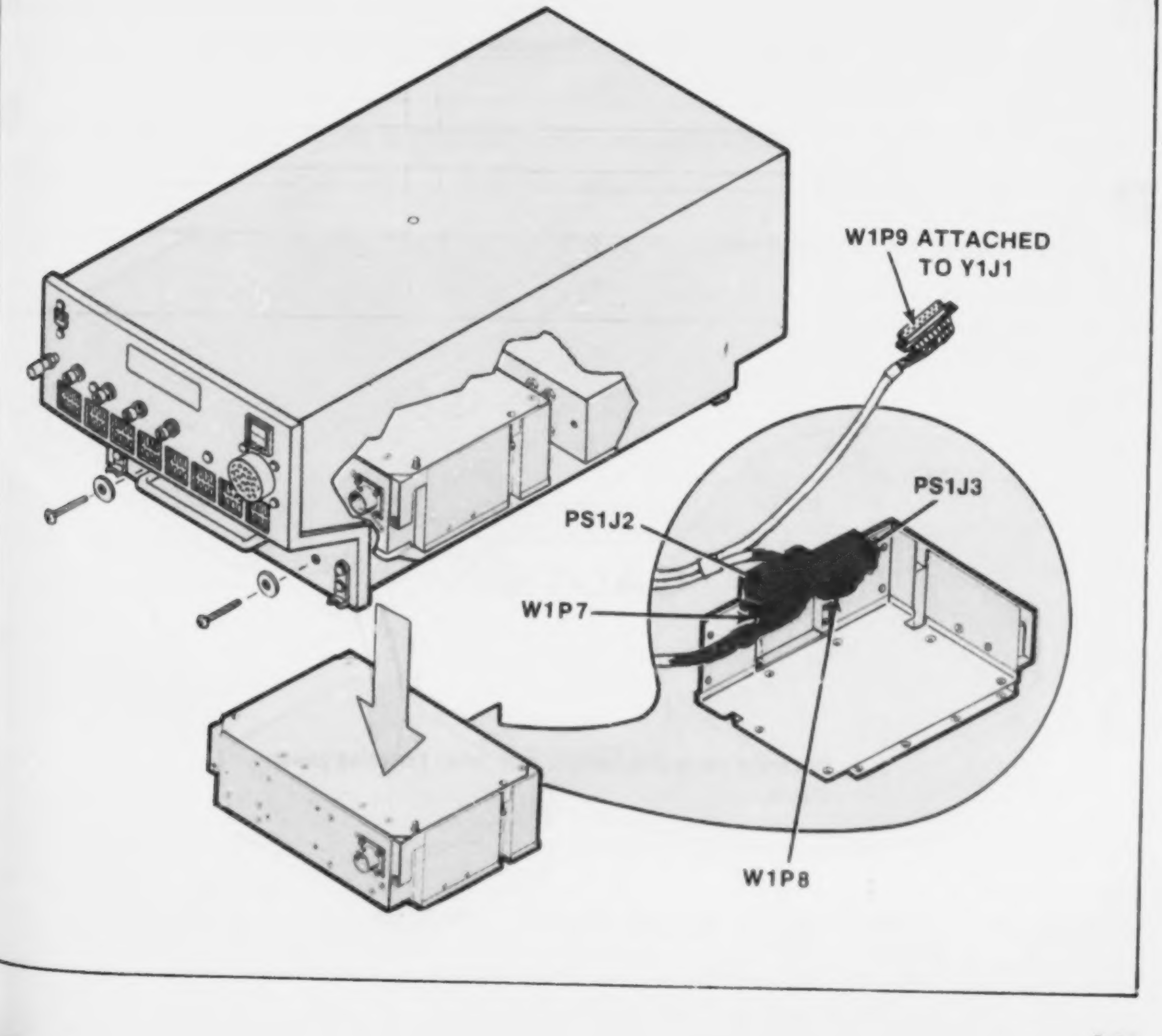
7 Torque connectors W14P2 and W16P2 to 8 in.-lbs.

3-20. REPLACEMENT OF POWER SUPPLY PS1

REMOVAL

1 Turn receiver transmitter to gain access to power supply.

2 Remove two screws and two flat washers securing power supply to front panel.


W1P9 ATTACHED TO Y1J1
PS1J3
PS1J2
W1P7
W1P8

3-20. REPLACEMENT OF POWER SUPPLY PS1 (Continued)

REMOVAL (Continued)

3

Loosen the two screws securing harness connector W1P9 to Y1J1. Disconnect connector.

4

Disconnect W1P8 from PS1J3 and W1P7 from PS1J2.

5

Loosen four captive screws (part of PS1) from threaded inserts in base of chassis.

6

Remove power supply from chassis.

CAUTION

Be careful not to skin harness cable when removing power supply.

3-20. REPLACEMENT OF POWER SUPPLY PS1

REPLACEMENT

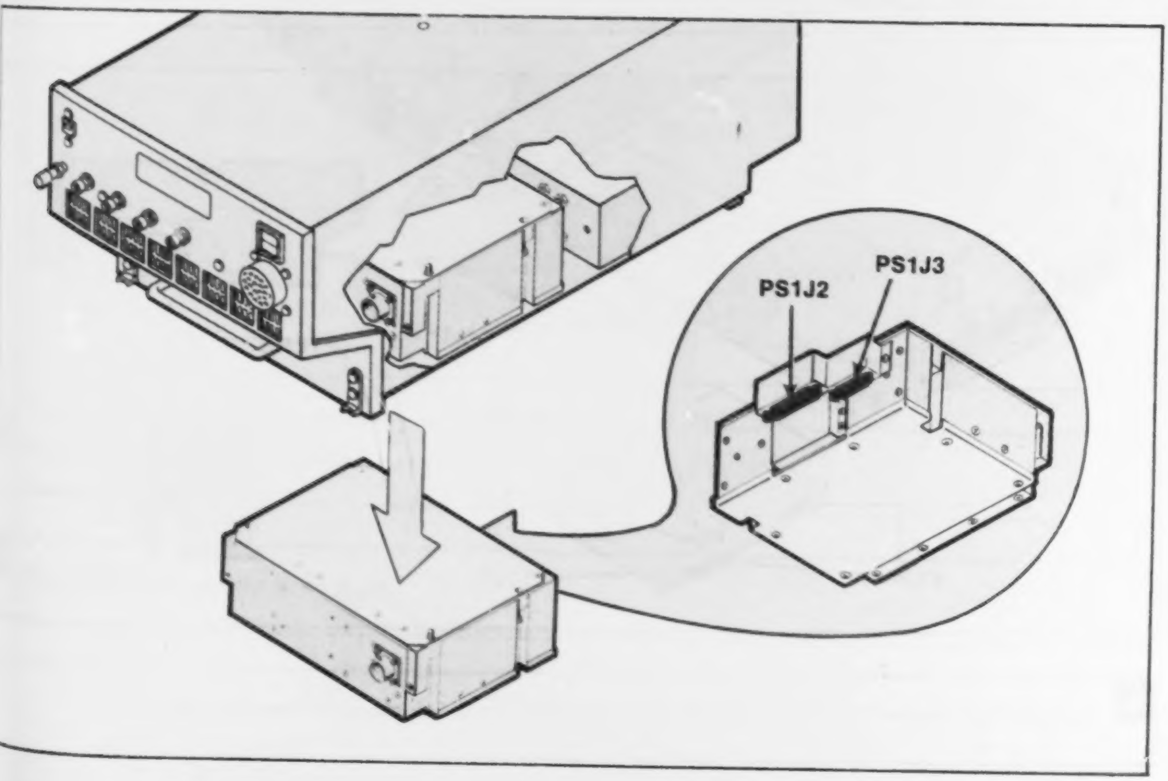
1 Place power supply into position in chassis.

2 Tighten four captive screws (part of power supply) to threaded inserts in chassis.

3 Replace two screws and two flat washers securing power supply to front panel of chassis.

4 Connect W1P8 to PS1J3 and W1P7 to PS1J2.

5 Connect cable connector W1P9 to Y1J1 and tighten connector screws.



3-21. REPLACEMENT OF FREQUENCY MULTIPLIER OSCILLATOR Y1

REMOVAL

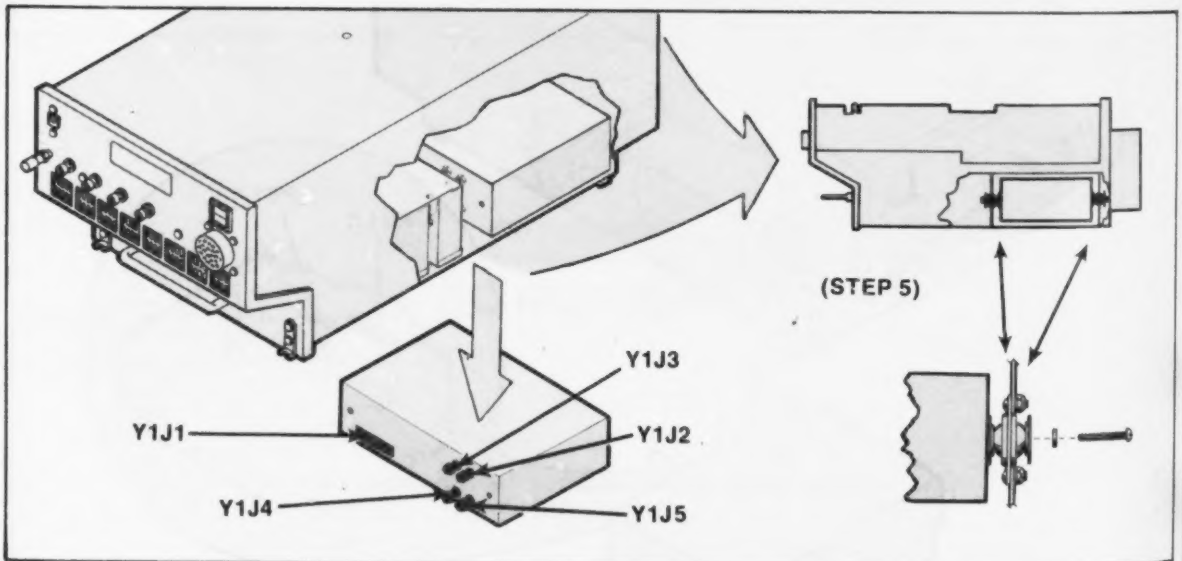
1 Turn receiver transmitter to gain access to FMO.

2 Remove power supply (para 3-20).

3 Loosen eight fasteners securing blower assembly to chassis. Move blower assembly away from chassis. (Refer to para 3-24).

4 Disconnect the following cable connectors from FMO connectors:

CABLE CONNECTOR	FMO CONNECTOR
W17P1	Y1J4
W10P1	Y1J5
W15P2	Y1J3
W13P1	Y1J2



5 Remove four screws and four washers securing FMO to shock mounts. Remove FMO.

3-21. REPLACEMENT OF FREQUENCY MULTIPLIER OSCILLATOR Y1 (Continued)

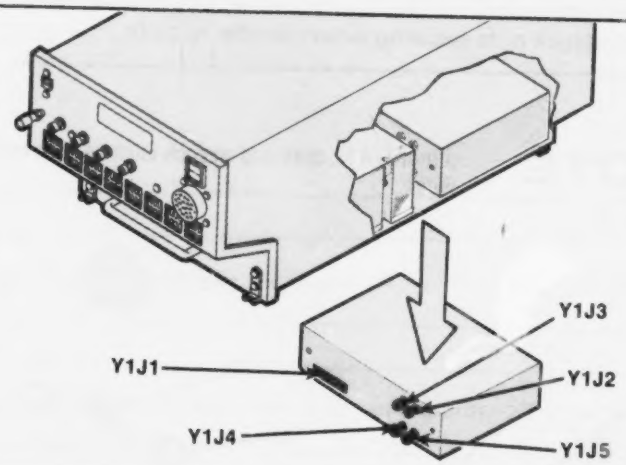
REPLACEMENT

1 Place FMO into position in chassis.

1 Replace four screws and four washers securing FMO to shock mounts.

3 Attach the following cable connectors to FMO connectors and torque to 8 in.-lbs:

CABLE CONNECTOR	FMO CONNECTOR
W13P1	A1J2
W15P1	Y1J3
W10P1	Y1J5
W17P1	Y1J4



4 Place blower assembly against chassis and secure with eight fasteners.

5 Replace power supply (para 3-20).

3-22. REPLACEMENT OF POWER DIVIDER A18.

REMOVAL

1 Remove first IF assembly (para 3-19).

2 Perform steps 1 through 5 of power amplifier removal procedure (para 3-24).

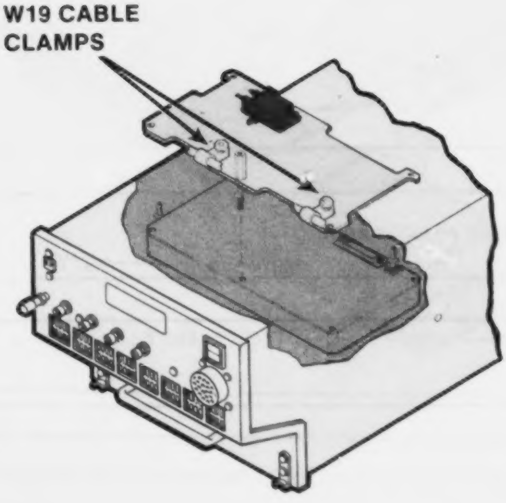
3 Remove two locking nuts and two flat washers securing cable W19 cable clamps to mounting plate.

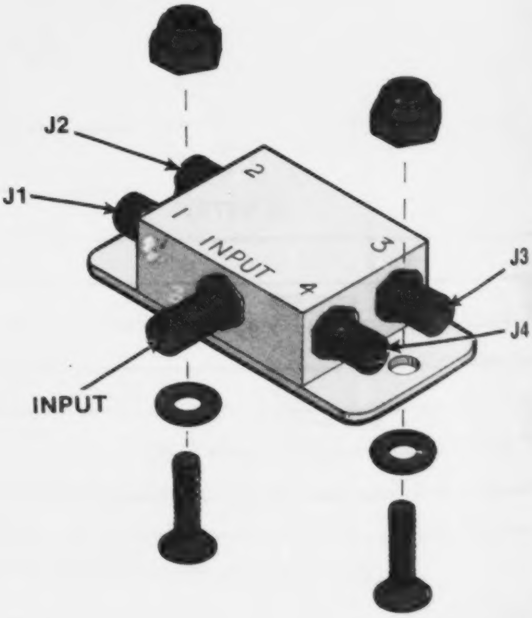
4 Disconnect cable connectors W10P2, W3P2, W6P2, W7P2 and W11P2 from power divider.

5 Tip mounting plate to the left and lift out of chassis.

6 Remove two screws and lock nuts securing power divider to plate.

NOTE **A thin 1/4 in. open end wrench must be used to hold locking nuts.**





3-22. REPLACEMENT OF POWER DIVIDER A18 (Continued)

REPLACEMENT

1 Attach power divider to mounting plate with two screws and two lock nuts.

2 Position mounting plate vertically over power amplifier and adjacent to cable W19.

3 Position cable clamps on to mounting plate screws and rotate mounting plate into horizontal position.

4 Attach the following cable connectors to the directional coupler connectors and torque to 8 in.-lbs:

CABLE CONNECTOR	COUPLER CONNECTOR
W10P2	INPUT
W3P2	J1
W6P2	J2
W7P2	J3
W11P2	J4

5 Replace two locking nuts and flat washers securing cable W19 cable clamps to mounting plate.

6 Perform steps 5 through 8 of power amplifier replacement procedure (para 3-24).

7 Replace first IF assembly (para 3-19).

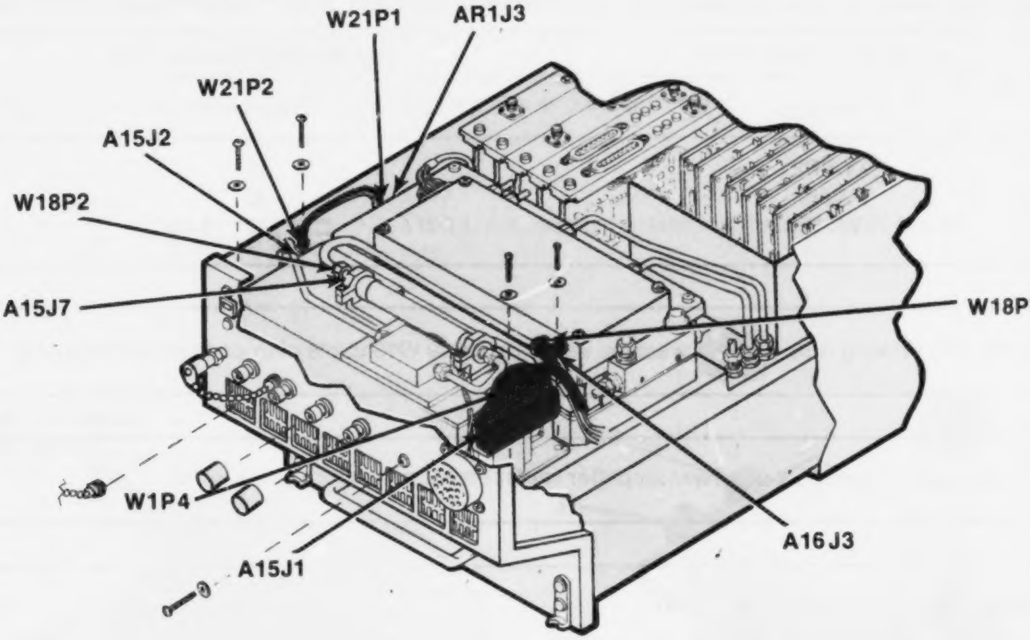
3-23. REPLACEMENT OF DUPLEXER A15

REMOVAL

1 Disconnect W18P1 from A16J3 and W18P2 from A15J7. Remove cable W18.

2 Loosen connector W21P1 from connector AR1J3.

3 Disconnect W21P2 from A15J2.


W21P1
AR1J3
W21P2
A15J2
W18P2
A15J7
W18P1
W1P4
A15J1
A16J3

4 Loosen two screws securing harness connector W1P4 to A15J1. Disconnect connectors.

5 Remove four screws and four flat washers securing duplexer to top of chassis.

3-23. REPLACEMENT OF DUPLEXER A15 (Continued)

REMOVAL (Continued)

6 Remove two screws, two lockwashers and two flat washers securing duplexer to front panel.

NOTE

Lug attached to chain connected to dummy load on front panel connector J7 will come off when screw nearest J3 is removed.

7 Remove protective caps from front panel connectors J5 and J6.

8 Loosen four screws attaching first IF assembly.

9 Raise front edge of first IF assembly slightly and remove duplexer.

CAUTION

Use care so as not to put excessive stress on hard-line cables

3-23. REPLACEMENT OF DUPLEXER A15 (Continued)

REPLACEMENT

1

Raise front edge of first IF assembly and place duplexer in its normai position on top of chassis.

NOTE

Lug attached to chain goes between lockwasher and flat washer.

2

Replace two screws, two lockwashers and two flat washers through front panel into duplexer.

3

Replace four screws and four flat washers attaching duplexer to top of chassis.

4

Tighten four screws attaching first IF assembly.

5

Connect cable connector W1P4 to A15J1 and tighten connector screws.

3-23. REPLACEMENT OF DUPLEXER A15 (Continued)

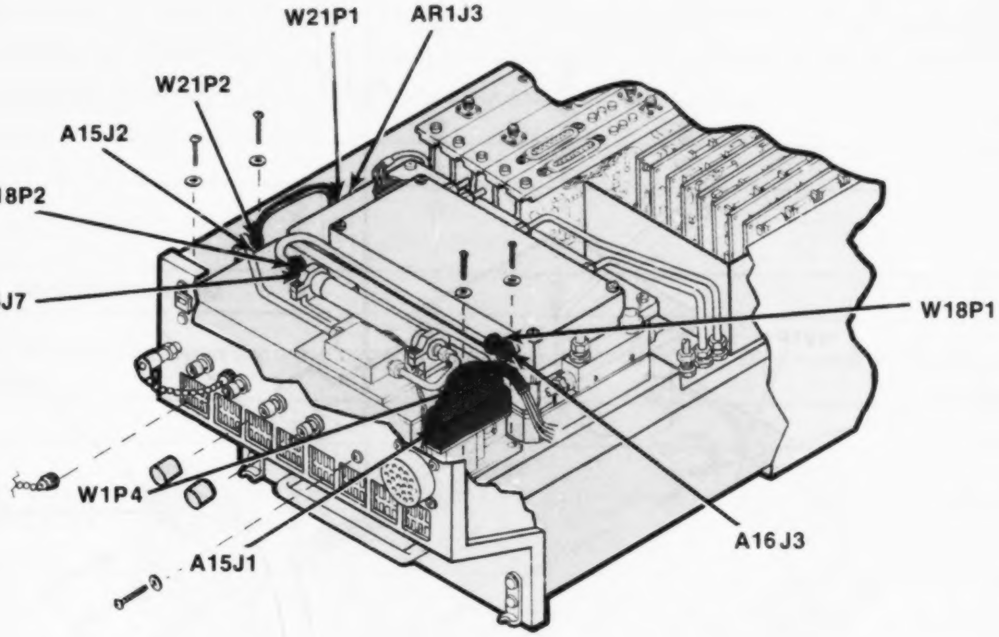
REPLACEMENT (Continued)

6

Connect cable connector W21P2 to A15J2. Torque W21P2 and W21P1 to 8 in.-lbs.

7

Place cable W18 in position and connect W18P1 to A16J3 and W18P2 to A15J7. Torque connectors to 8 in.-lbs.


W21P1
AR1J3
W21P2
A15J2
W18P2
A15J7
W18P1
W1P4
A15J1
A16 J3

8

Replace protective caps on front panel connector J5 and J6.

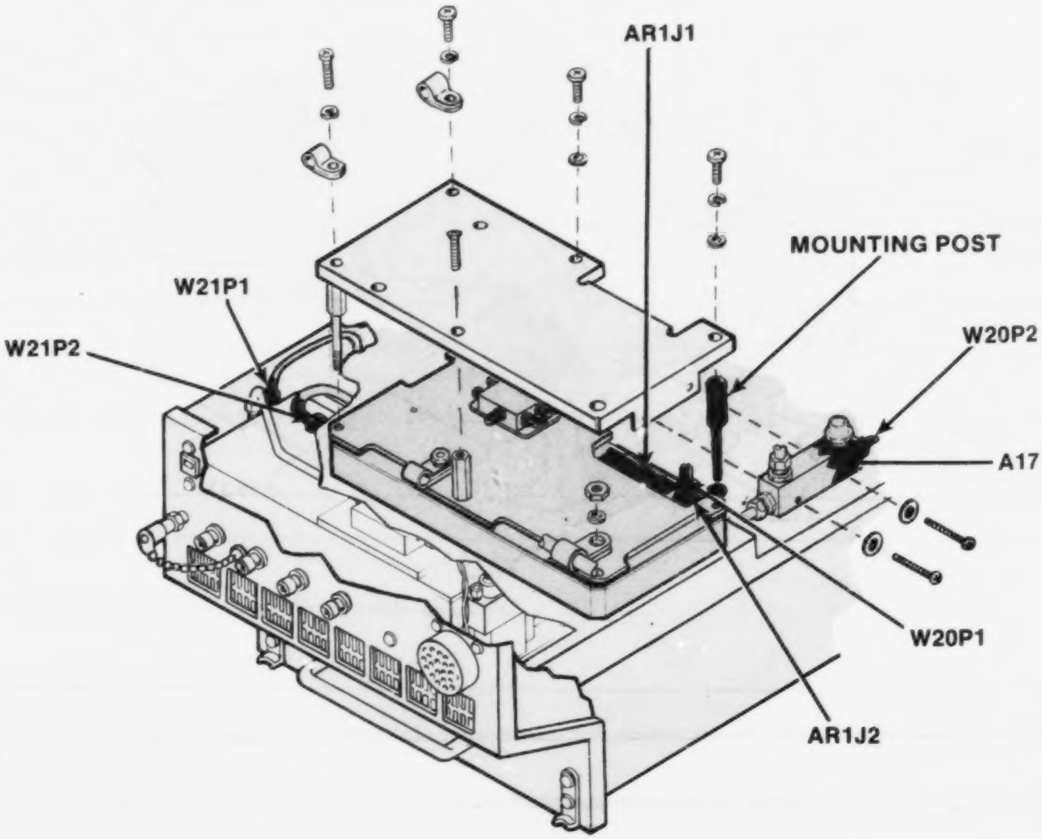
3-24. REPLACEMENT OF POWER AMPLIFIER AR1

REMOVAL

1 Remove first IF assembly (para 3-19).

2 Remove two screws and lockwashers attaching directional coupler A17 to first IF assembly mounting bracket.

3 Remove one flat head screw and four pan head screws, four lockwashers, and four flat washers securing mounting bracket to spacers. Remove mounting bracket.


AR1J1
MOUNTING POST
W21P1
W21P2
W20P2
A17
W20P1
AR1J2

3-24. REPLACEMENT OF POWER AMPLIFIER AR1 (Continued)

REPLACEMENT (Continued)

4 Cut and remove lacing securing cables to two mounting posts.

5 Remove the six mounting posts and six flat washers.

6 Loosen connector W20P2 from directional coupler connector A17.

7 Disconnect W20P1 from AR1J2.

8 Loosen connector W21P2 from duplexer connector A15J2.

9 Disconnect W21P1 from AR1J3.

10 Loosen two captive screws securing harness connector W1P5 to AR1J1. Disconnect connectors.

11 Remove power amplifier from chassis by sliding out to the left from under directional coupler mounting plate.

NOTE

Raise and tilt directional coupler mounting plate while removing power amplifier.

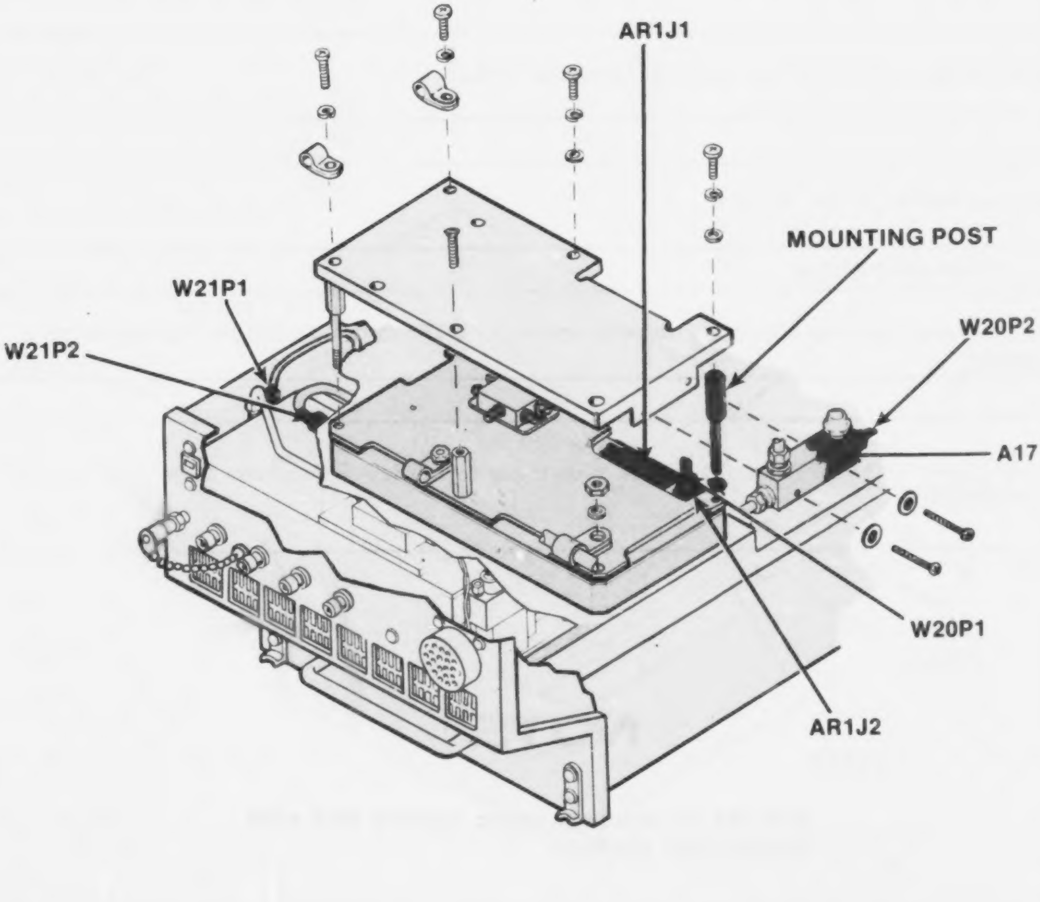
3-24. REPLACEMENT OF POWER AMPLIFIER AR1 (Continued)

REPLACEMENT

1 Slide power amplifier into position under directional coupler mounting plate and align holes in plate with holes in power amplifier.

2 Connect cable connector W1P5 to AR1J1 and tighten connector screws.

3 Connect cable connectors W21P2 to AR1J3 and W20P1 to AR1J2. Torque connectors to 8 in.-lbs.


AR1J1
MOUNTING POST
W21P1
W20P2
W21P2
A17
W20P1
AR1J2

-24. REPLACEMENT OF POWER AMPLIFIER AR1 (Continued)

EMOVAL (Continued)

4 Torque connectors W21P1 and W20P2 to 8 in.-lbs.

5 Replace six mounting posts and six flat washers securing mounting plate and power amplifier to chassis.

6 Secure cabling to right front and back mounting posts with lacing cord.

Position first IF mounting plate over mounting posts and secure with four pan head screws, four lockwashers and four flat washers, and one flat head screw.

NOTE

Ensure that the two cable clamps are secured by the two left screws.

Replace two screws and lock washers securing directional coupler A17 to edge of first IF mounting bracket.

Remove first IF assembly (para 3-19).

3-25. REPLACEMENT OF BLOWER ASSEMBLY B1

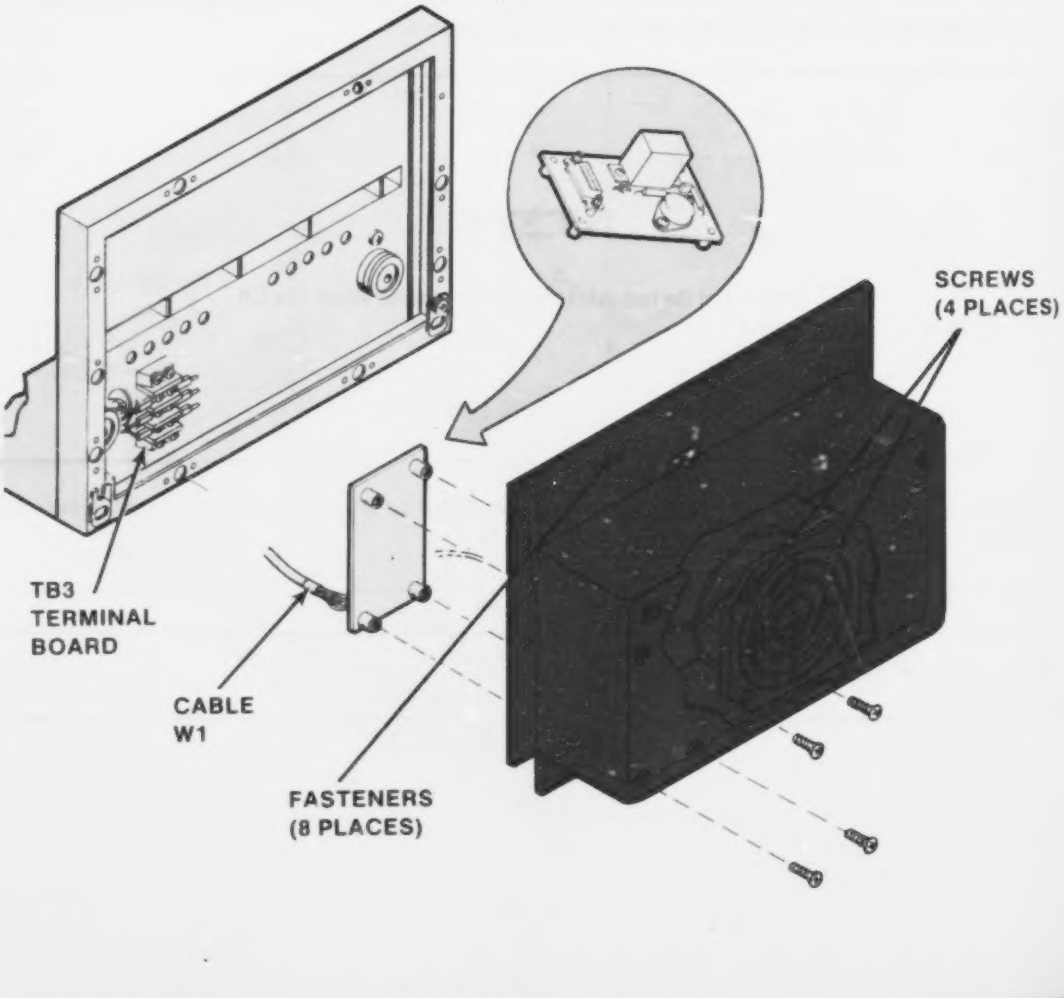
REMOVAL

1. Loosen eight fasteners securing blower assembly to chassis. Move blower assembly away from chassis.

2. Untie lacing cord ties securing blower cable to cable W1.

3. Disconnect blue, red, and yellow blower leads from terminal board TB3 by removing terminal board screws.

4. Loosen four screws and eccentric clamps securing blower to mounting plate. Remove blower with blower cable.


SCREWS
(4 PLACES)
TB3
TERMINAL
BOARD
CABLE
W1
FASTENERS
(8 PLACES)

3-25. REPLACEMENT OF BLOWER ASSEMBLY B1 (Continued)

REPLACEMENT

1 Place replacement blower in position on inside of blower assembly.

2 Tighten four screws and clamps to secure blower.

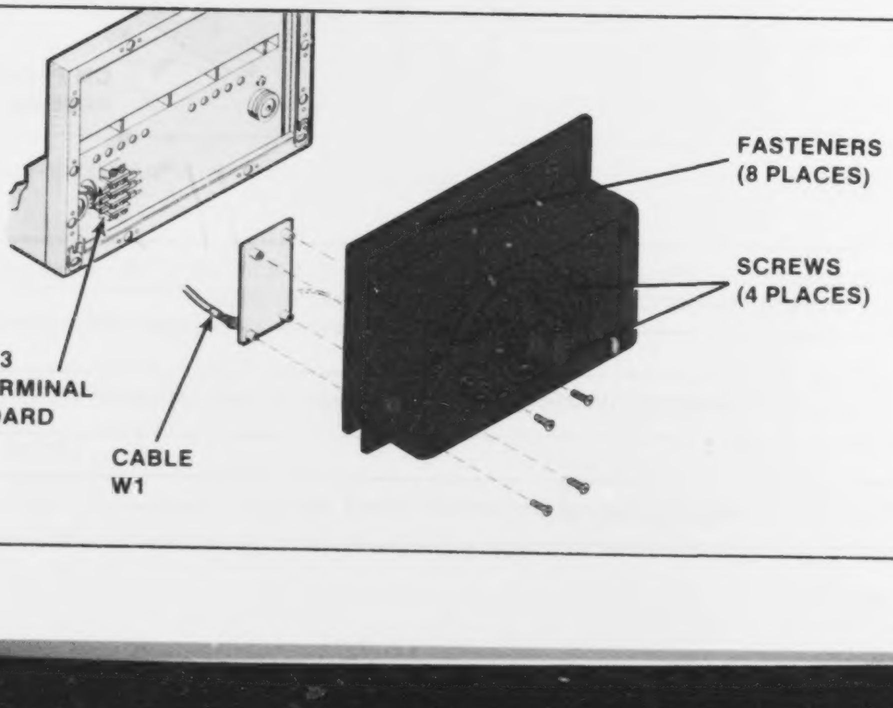
NOTE Eccentric clamps will position themselves over edge of blower as screws are tightened.

3 Connect blower leads to terminal board TB3.

NOTE Blower will run backwards if leads are connected incorrectly. Blue lead is connected to TB3-A, red lead is connected to TB3-B, and yellow lead is connected to TB3-C.

4 Secure blower cable to cable W1 with lacing cord.

5 Place blower assembly against chassis and secure with eight fasteners.



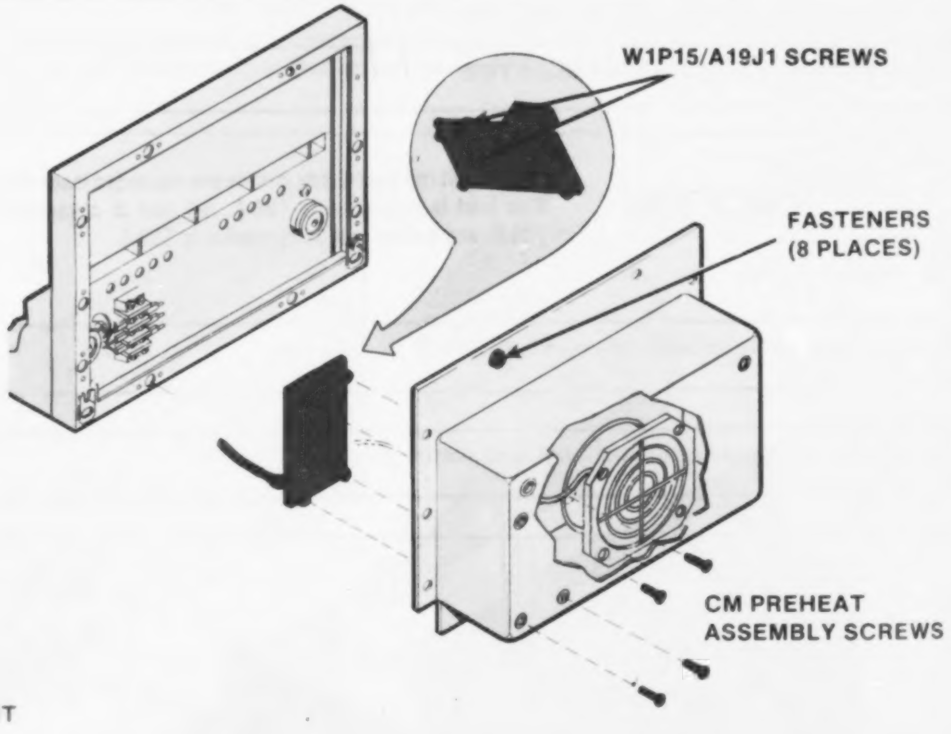
3-26. REPLACEMENT OF CM PREHEAT ASSEMBLY A19

REMOVAL

1 Loosen eight fasteners securing blower assembly to chassis. Move blower assembly away from chassis.

2 Loosen two screws securing harness connector W1P15 to A19J1. Disconnect connector.

3 Remove four screws securing CM preheat assembly and remove preheat assembly.



REPLACEMENT

1 Apply compound MS22473G4-A (Item 7, Appendix B, Section II) to four screws. Insert and tighten four screws to secure CM preheat assembly to blower assembly.

2 Connect cable connector W1P15 to A19J1 and tighten connector screws.

3 Place blower assembly against chassis and secure with eight fasteners.

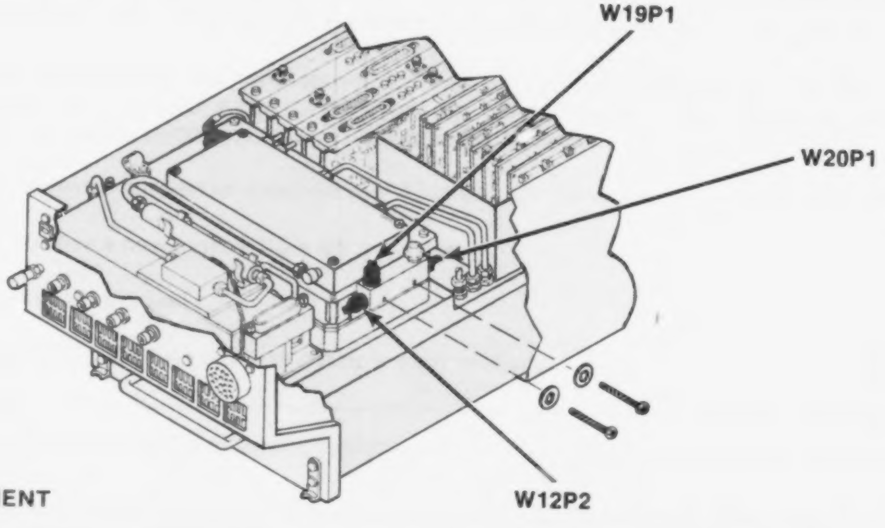
-27. REPLACEMENT OF DIRECTIONAL COUPLER A17

REMOVAL

1 Disconnect the following cable connections.

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W19P1	-30 DB OUTPUT
W12P1	IN
W20P1	OUT

2 Remove the two screws and lockwashers attaching directional coupler to first IF assembly mounting plate. Remove coupler.



REPLACEMENT

1 Secure directional coupler to edge of first IF assembly mounting plate with two screws and lockwashers.

2 Make the following cable connections and torque to 8 in. - lbs.

CABLE CONNECTOR	ASSEMBLY CONNECTOR
W20P2	OUT
W12P1	IN
W19P1	-30 DB OUTPUT

CHAPTER 4
MAINTENANCE INSTRUCTIONS FOR CONTROL INDICATOR

SECTION I.
CONTROL INDICATOR CHECK PROCEDURE

SECTION CONTENTS	PAGE
GENERAL	4-1
TEST SETUP INTERCONNECTIONS	4-1
INITIAL SWITCH POSITIONS	4-2
TEST PROCEDURE	4-2

4-1. GENERAL

This section contains a check procedure which will permit you to determine if the control indicator is operating correctly. To test a control indicator, you must connect it into a test setup using the test set TS-3609. You should perform a control indicator check when:

- You receive a suspected defective unit from unit maintenance
- You receive a new system from army supply
- After repair of a unit
- Anytime you suspect a unit is not operating properly

4-2. TEST SETUP INTERCONNECTIONS

Connect the control indicator to the test set as shown in figure 4-1 using test cables supplied with the test set.

CAUTION

Ensure that the 115V 400 Hz power is not activated when connecting power cable W1 to the test set.

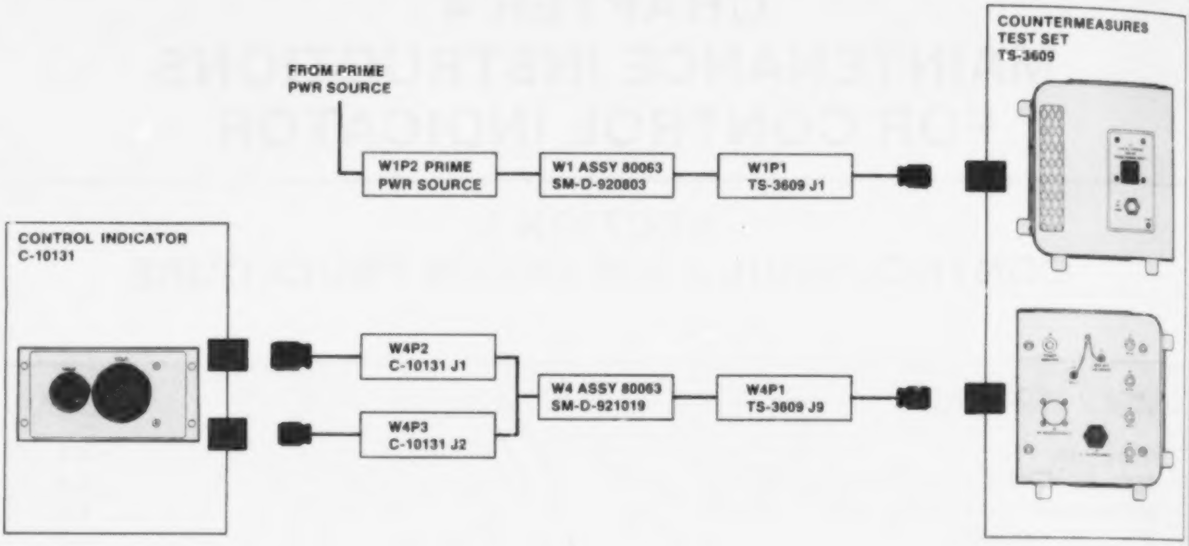

FROM PRIME PWR SOURCE
W1P2 PRIME PWR SOURCE
W1 ASSY 80063 SM-D-920803
W1P1 TS-3609 J1
COUNTERMEASURES TEST SET TS-3609
CONTROL INDICATOR C-10131
W4P2 C-10131 J1
W4P3 C-10131 J2
W4 ASSY 80063 SM-D-921019
W4P1 TS-3609 J9

Figure 4-1. Control Indicator and Test Set Interconnections

4-3. INITIAL SWITCH POSITIONS

Set the POWER switch on the control indicator to OFF. Actuate the PUSH FOR STANDBY switch to its out (normal) position.

Set the switches on the test set to their OFF, NORM (or NORMAL), fully counterclockwise or lowest numbered positions. Set the FMO PHASE CODE and BITE switches to OFF.

4-4. TEST PROCEDURE

Check the control indicator by performing the steps listed in the OPERATION column of the following chart. If you do not obtain the normal indication, refer to the CORRECTIVE ACTION column for instructions.

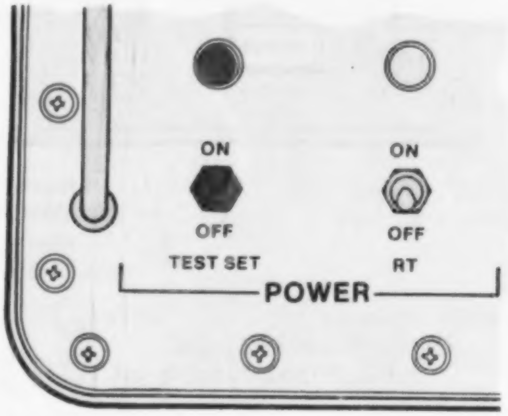
If, after performing the corrective action, you are still unable to obtain a specified normal indication, refer to the functional diagrams and description given in Section II of Chapter 2. Use the ohmmeter to check wiring associated with the problem you are experiencing, and repair the wiring if required. Read the circuit description as it will help you understand the operation of the control indicator, and may aid you in locating a defective component.

If you cannot correct the problem, return the control indicator to a higher category of maintenance for repair.

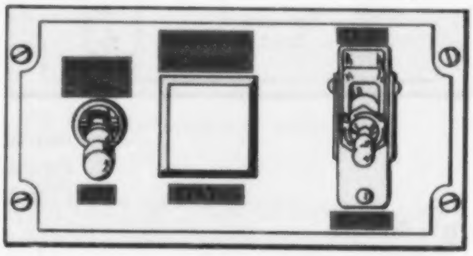
TEST PROCEDURES (Continued)

STEP	OPERATION → NORMAL INDICATION → CORRECTIVE ACTION
1.	Energize the 115 V, 400 Hz power source.
2.	(TS) TEST SET POWER: ON

(TS) TEST SET POWER indicator lights.



(CI) Front panel engraving lights.



NOTE

Unless the room can be darkened, it will be necessary to view the control indicator under a dark cover for you to see the illuminated engraving.

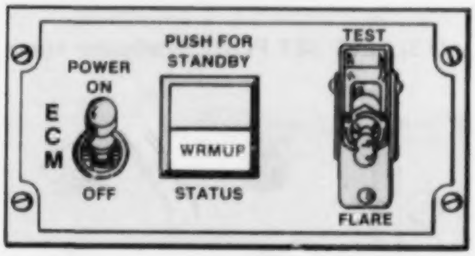
Replace illuminated panel (para 4-6)

TEST PROCEDURES (Continued)

STEP | **OPERATION** → **NORMAL INDICATION** → **CORRECTIVE ACTION**

3. (CI) POWER: ON

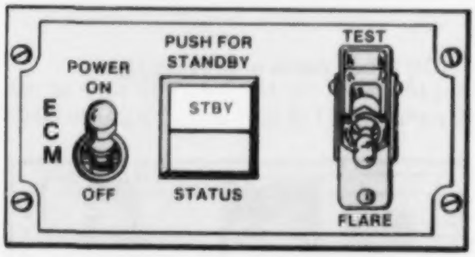
(CI) WRMUP indicator lights.


PUSH FOR STANDBY
TEST
POWER ON
ECM
WRMUP
OFF
STATUS
FLARE

Replace S1 (POWER switch) or A1 (para 4-5).
Replace indicator lamps (TM 11-5865-201-12).

4. (CI) PUSH FOR STANDBY: Depress

(CI) STBY indicator lights.
WRMUP indicator goes out.

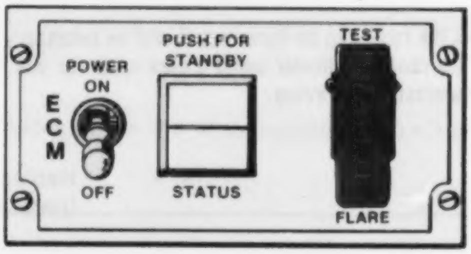

PUSH FOR STANDBY
TEST
POWER ON
ECM
STBY
OFF
STATUS
FLARE

Replace S2 (STATUS switch).
Replace indicator lamps (TM 11-5865-201-12).

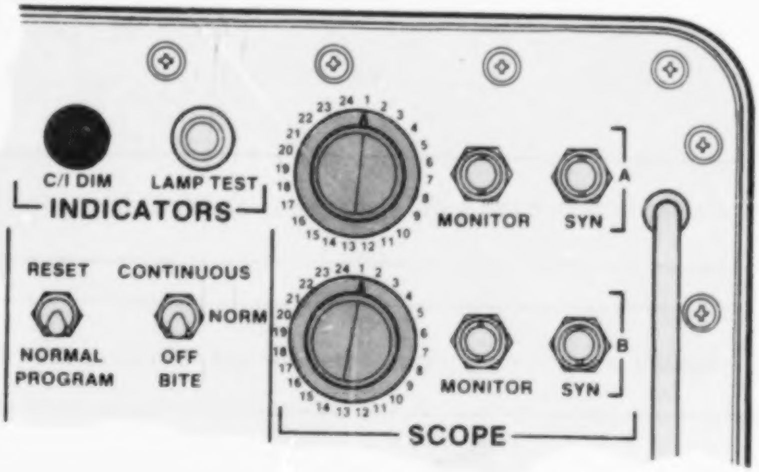
5. (CI) PUSH FOR STANDBY: Release

(CI)STBY indicator goes out.
WRMUP indicator lights

6. (CI) FLARE TEST: Set to ON position (up) momentarily.


PUSH FOR STANDBY
TEST
POWER ON
ECM
OFF
STATUS
FLARE

TEST PROCEDURES (Continued)

STEP	OPERATION	NORMAL INDICATION	CORRECTIVE ACTION
		(TS) STBY, CM INOP and CM JAM indicators light.	Replace S3 (FLARE TEST switch) or A1 (para 4-5).
7.	(TS) C/I DIM: Depress momentarily.		
	 C/I DIM LAMP TEST INDICATORS RESET NORMAL CONTINUOUS NORM OFF BITE PROGRAM MONITOR SYN A MONITOR SYN B SCOPE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24		
		(CI) WRMUP indicator dims. Replace A1 (Par. 3-5)	Replace A1 (para 4-5).
8.	(CI) POWER: OFF	(CI) WRMUP indicator goes out.	
9.	(TS) TEST SET POWER: OFF	(TS) TEST SET POWER indicator goes out.	
10.	Disconnect test cables and place in storage within test set.		

SECTION II.
CONTROL INDICATOR DISASSEMBLY AND ASSEMBLY

ECTION CONTENTS **PAGE**

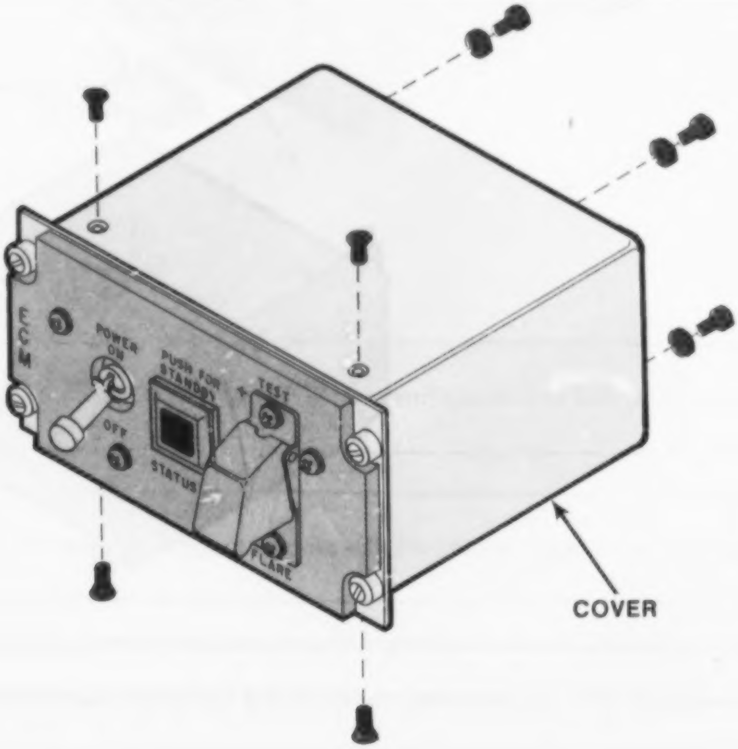
EPLACEMENT OF CIRCUIT CARD ASSEMBLY 1A2A1 4-7
EPLACEMENT OF ILLUMINATED FRONT PANEL 4-10

REPLACEMENT OF CIRCUIT CARD ASSEMBLY 1A2A1

MOVAL

Remove four, flat phillips-head screws securing cover to top and bottom of chassis.

Remove four round head screws and four washers securing cover to rear of chassis. Remove cover.

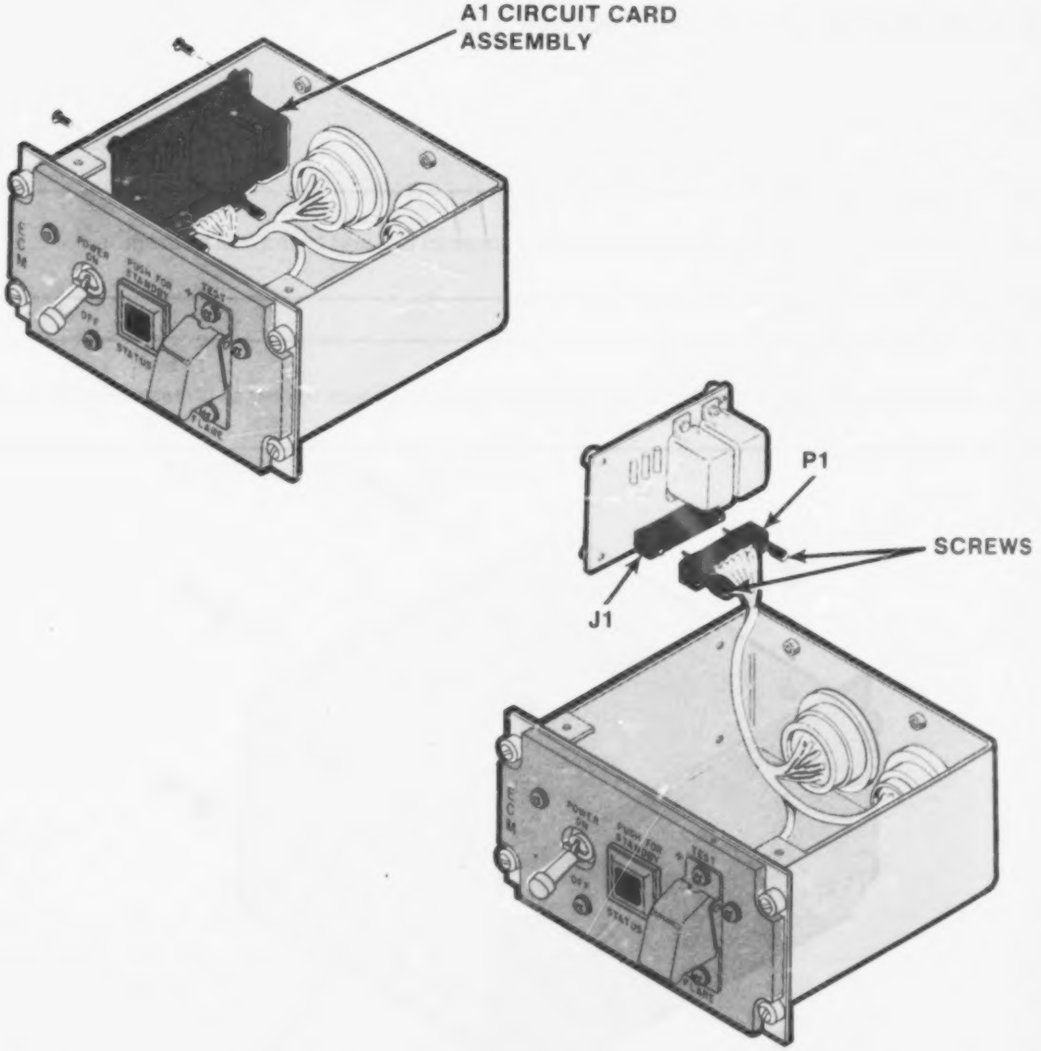

E C M
POWER ON
OFF
PUSH FOR STANDBY
STATUS
TEST
FLARE
COVER

4-5. REPLACEMENT OF CIRCUIT CARD ASSEMBLY 1A2A1 (Continued)

REMOVAL (Continued)

3

Remove four flat phillips-head screws securing A1 circuit card assembly to left side of chassis. Move card assembly and attaching harness out of chassis in order to gain access to harness connector P1.


A1 CIRCUIT CARD ASSEMBLY
ECM
POWER ON
OFF
PUSH FOR STANDBY
STATUS
TEST
FLARE
P1
SCREWS
J1

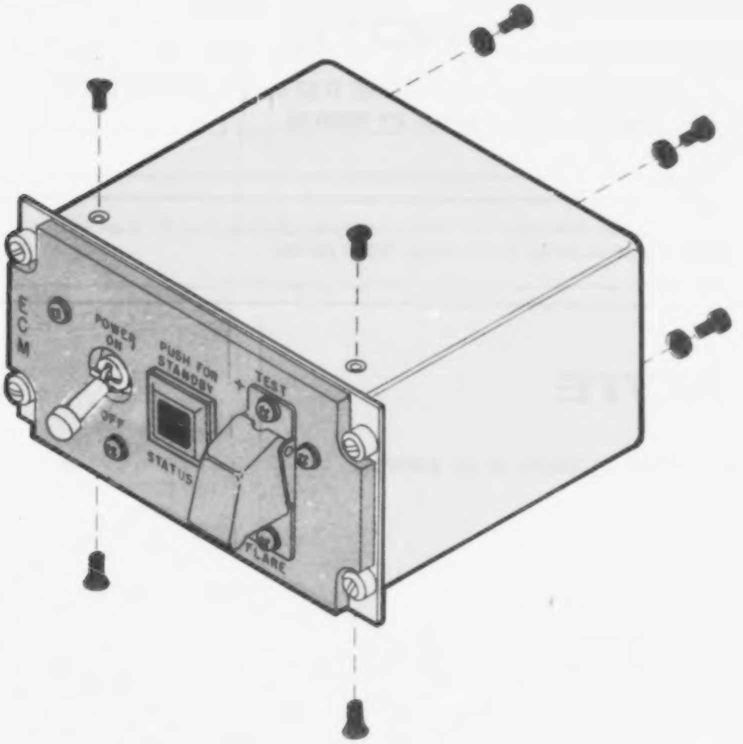
4

Disconnect connector P1 from card assembly, by loosening two screws securing P1 to J1.

4-5. REPLACEMENT OF CIRCUIT CARD ASSEMBLY 1A2A1 (Continued)

REPLACEMENT

1 Connect harness connector P1 to A1J1 and tighten connector screws.


ECM
POWER ON
OFF
PUSH FOR STANDBY
STATUS
TEST
FLARE

2 Position A1 circuit card assembly within chassis and secure with four phillips-head screws.

3 Replace cover and secure to rear of chassis with four round head screws and washers.

4 Replace four flat phillips screws on top and bottom of cover.

4-6. REPLACEMENT OF ILLUMINATED FRONT PANEL

REMOVAL

1 Remove seven screws, seven lockwashers, and seven flat washers securing illuminated panel to inner panel.

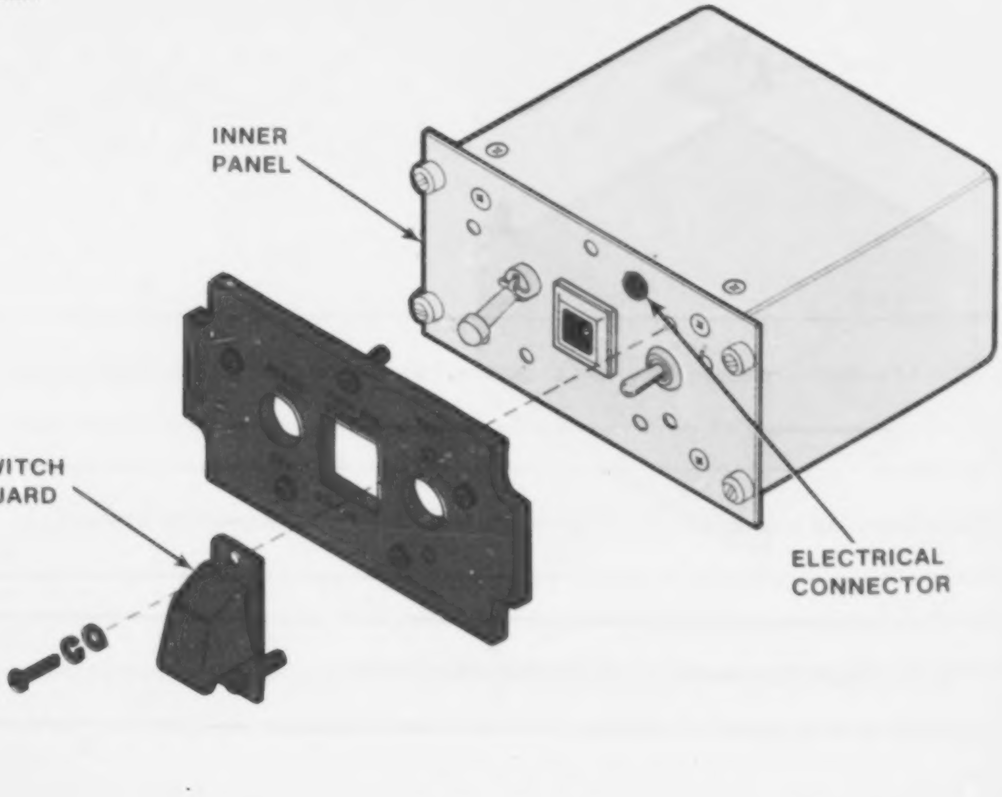
NOTE

The switch guard for the FLARE TEST switch will come off when two of these screws are removed.

2 Gently pull illuminated panel away from inner front panel.

NOTE

The two panels are attached by means of an electrical connector.


INNER PANEL
SWITCH GUARD
ELECTRICAL CONNECTOR

4-6. REPLACEMENT OF ILLUMINATED FRONT PANEL (Continued)

REPLACEMENT

1 Position new illuminated front panel over inner front panel and press together so that electrical connectors mate.

2 Place switch guard over FLARE TEST switch and secure with two sets of the screws, lockwashers and flat washers removed in step 1.

3 Replace remaining five sets of screws lockwashers and flat washers removed in step a.

APPENDIX A
REFERENCES

A-1. PUBLICATION INDEXES

The following indexes should be consulted frequently for latest changes or revisions of references given in this appendix and for new publications relating to material covered in this manual.

Consolidated Index of Army Publications and Blank Forms .... DA Pam 310-1

A-2. FORMS AND RECORDS

Recommended Changes to Equipment Technical Publications .... DA Form 2028-2

The following forms and records pertain to this material.

Discrepancy in Shipment Report .... SF 361

Report of Discrepancy .... SF 364

Quality Deficiency Report .... SF 368

A-3. OTHER PUBLICATIONS

The following publications contain information pertinent to this material and associated equipment.

DESTRUCTION TO PREVENT ENEMY USE

Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command) .... TM 750-244-2

GENERAL

Preservation, Packaging and Packing Material, Supplies and Equipment Used by Army .... SB 38-100

The Army Maintenance Management System (TAMMS) .... TM 38-750

MAINTENANCE

Administrative Storage Requirements .... TM 740-90-1

RELATED PUBLICATIONS

Packaging and Handling .... AR 700-58

Army Shipping Documents .... AR 725-5

RELATED PUBLICATIONS (Cotninued)

Organizational Maintenance Manual Electronic Equipment Configuration Army Model CH-47A (NSN 1520-00-633-6836), CH-47B (NSN 1520-000-990-2941) and CH-47C (NSN 1520-00-871-7308) Helicopters	TM 11-1520-209-20
Aviation Unit Maintenance Manual Electronic Equipment Configuration Army Model CH-47D Helicopter (NSN 1520-01-088-3669)	TM 11-1520-240-20
Aviation Unit Maintenance Manual For Countermeasures Set AN/ALQ-156(V)1 (NSN 5865-01-145-5197)	TM 11-5865-201-12
Aviation Unit Maintenance Repair Parts and Special Tool List for Countermeasures Set AN/ALQ1-56(V)1 (NSN 5865-01-145-5197)	TM 11-5865-201-20P
Aviation Intermediate Maintenance Repair Parts and Special Tools Lists (Including Depot Maintenance Repair Parts and Special Tools) for Countermeasures Set AN/ALQ-156(V)1 (NSN 5865-01-145-5197)	TM 11-5865-201-30P
Aviation Intermediate Maintenance Manual for Countermeasures Set AN/ALQ-156(V)1 (Classified Supplement to TM 11-5865-201-30-1) (NSN 5865-01-145-5197	TM 11-5865-201-30-2
Operator's Aviation Unit, and Intermediate Maintenance Manual for Countermeasures Test Set TS-3609/ALQ-156(V) (NSN 6625-01-142-3433)	TM 11-6625-2883-13
Hand Receipt Manual for Countermeasures Test Set TS-3609/ALQ-156(V) (NSN 6625-01-142-3433)	TM 11-6625-2883-13HR
Aviation Unit and Intermediate Maintenance Repair Parts and Special tools Lists (Including Depot Maintenance Repair Parts and Special Tools) for Countermeasures Test Set TS-3609/ALQ-156(V) (NSN 6625-01-142-3433)	TM 11-6625-2883-23P

APPENDIX B
EXPENDABLE SUPPLIES AND MATERIALS LIST

SECTION I.
INTRODUCTION

B-1. SCOPE

This appendix lists expendable supplies and materials you will need to operate and maintain the AN/ALQ-156 (V)1 system. These items are authorized to you by CTA 50-970. Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items)

B-2. EXPLANATION OF COLUMNS

a. Column 1 - Item number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e.g., 'Use cleaning compound, item 6, App. B')

b. Column 2 - Level. This column identifies the lowest level of maintenance that requires the listed item.

C - Operator/Crew

O - Organizational Maintenance (AVUM)

F - Direct Support (AVIM)

c. Column 3 - National Stock Number. This is the National stock number assigned to the item; use it to request or requisition the item.

d. Column 4 - Description. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the Federal Supply Code for Manufacturer (FSCM) in parentheses followed by the part number.

e. Column 5 - Unit of Measure (U/M). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

SECTION II
EXPENDABLES SUPPLIES AND MATERIALS LIST

(1) ITEM NUMBER	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION	(5) U/M
1	O		Sealant, Dow Corning 732-3RTV or equivalent	A/R
2	O		Wire, Safety	A/R
3	O		Cloth, lint-free, cleaning	A/R
4	O		Brush, paint	EA
5	F	3439-00-555-4629	Solder	AR
6	C, F	6850-00-033-8851	Trichlorotrifluroethane	5 gal
7	F		Compound; Sealing, Locking and Retaining; Grade A (MIL-S-22473)	A/R

APPENDIX C
GLOSSARY OF NON-STANDARD ABBREVIATIONS (MNEMONIC CODES)

ABBREVIATION	DEFINITION
ACFT 28VS	AIRCRAFT 28V SWITCHED
ADISL	ANTENNA DISABLE LOW
ALOPWRH	ANTENNA LOW POWER HIGH
ANTD	ANTENNA DRIVE
ANT 1	ANTENNA 1
ANT 2	ANTENNA 2
APOSLSB	ANTENNA POSITION LEAST SIGNIFICANT BIT
APOSMSB	ANTENNA POSITION MOST SIGNIFICANT BIT
BBITEH	BUFFERED BITE HIGH
BDMPL	BUFFERED DUMP LOW
BENAL	BUFFERED ENABLE LOW
BITEH	BUILT IN TEST HIGH
BLLPWRH	BUFFERED LATCH LOW POWER HIGH
BRG1 ALARML	BUFFERED RANGE GATE 1 ALARM LOW
BRG2 ALARML	BUFFERED RANGE GATE 2 ALARM LOW
BRG3 ALARML	BUFFERED RANGE GATE 3 ALARM LOW
BSYNFL	BUFFERED SYNC FAULT LOW
BT0H	BUFFERED TIME ZERO HIGH
CM	COUNTERMEASURES
CM INOP	COUNTERMEASURES INOPERATIVE
CML	COUNTERMEASURES LOW
DIML	DIM LOW
DMPL	DUMP LOW
ECM	ELECTRONIC COUNTERMEASURES
ECMR	ELECTRONIC COUNTERMEASURES RESET
ECM1L	ELECTRONIC COUNTERMEASURES ONE LOW
ECM2L	ELECTRONIC COUNTERMEASURES TWO LOW
ECM3L	ELECTRONIC COUNTERMEASURES THREE LOW
FLTL	FAULT LOW
FLTN0H	FILTER NO. ZERO HIGH
FLTN1H	FILTER NO. ONE HIGH
FLTN2H	FILTER NO. TWO HIGH
FLTN3H	FILTER NO. THREE HIGH
FLTN4H	FILTER NO. FOUR HIGH

ABBREVIATION	DEFINITION
F0	TRANSMITTED RF FREQUENCY
F1	LOCAL OSCILLATOR FREQUENCY 1
F2	LOCAL OSCILLATOR FREQUENCY 2
F3	LOCAL OSCILLATOR FREQUENCY 3
INHBCLK	INHIBIT CLOCK
INH4L	INHIBIT FOUR MILLISECONDS LOW
INRSTL	INHIBIT RESET LOW
INHTX1L	INHIBIT TRANSMITTER ONE LOW
INHTX2L	INHIBIT TRANSMITTER TWO LOW
INXMTH	INHIBIT TRANSMITTER HIGH
JAMH	JAM HIGH
JAML	JAM LOW
LLPWRH	LATCH LOW POWER HIGH
LSDL	LARGE SIGNAL DETECTOR LOW
LSDLL	LARGE SIGNAL DETECTOR LATCHED LOW
MBBLH	MAINBANG BLANKING PULSE HIGH
MIC1L	MUTUAL INTERFERENCE COMPARATOR ONE LOW
MIENL	MUTUAL INTERFERENCE ENABLE LOW
MIL	MUTUAL INTERFERENCE LOW
PAON	POWER AMPLIFIER ON
PDMPH	PROCESSOR DUMP HIGH
PHASE	PHASE CODE
PROC PS FLTH	PROCESSOR/POWER SUPPLY FAULT HIGH
PROFLTH	PROCESSOR FAULT HIGH
PSFLTH	POWER SUPPLY FAULT
RF	SIG RF SIGNAL
RG1	RANGE GATE 1
RG2	RANGE GATE 2
RG3	RANGE GATE 3
RG1DAT	RANGE GATE ONE DATA SIGNAL (LIMITED)
RG2DAT	RANGE GATE TWO DATA SIGNAL (LIMITED)
RG3DAT	RANGE GATE THREE DATA SIGNAL (LIMITED)
RSTL	RESET LOW
SFRQ1H	STAMO FREQUENCY ONE HIGH
SFRQ2H	STAMO FREQUENCY TWO HIGH
SFRQ4H	STAMO FREQUENCY FOUR HIGH
SFRQ8H	STAMO FREQUENCY EIGHT HIGH
SFRQ16H	STAMO FREQUENCY SIXTEEN HIGH
SWFLTH	SWITCH FAULT HIGH

ABBREVIATION	DEFINITION
SWFLTDISH	SWITCH FAULT DIASABLE HIGH
SYNL	SYNC LOW
SYRSTL	SYSTEM RESET LOW
SYNFL	SYNC FAULT LOW
TOUTH	TIME OUT HIGH
TST1L	TEST ONE LOW
TST2L	TEST TWO LOW
TXONL	TRANSMITTER ON LOW
T0H	TIME ZERO HIGH
VSWRFLTH	VSWR FAULT HIGH
VSWRFLTL	VSWR FAULT LOW
WRMUPL	WARMUP LOW
XMIT+	TRANSMIT PULSE PLUS
XMIT-	TRANSMIT PULSE MINUS
0PRT0	PORT ZERO BIT ZERO
0PRT1	PORT ZERO BIT ONE
0PRT2	PORT ZERO BIT TWO
0PRT3	PORT ZERO BIT THREE
0PRT4	PORT ZERO BIT FOUR
0PRT5	PORT ZERO BIT FIVE
0PRT6	PORT ZERO BIT SIX
0PRT7	PORT ZERO BIT SEVEN
1PRT0	PORT ONE BIT ZERO
1PRT1	PORT ONE BIT ONE
1PRT2	PORT ONE BIT TWO
1PRT3	PORT ONE BIT THREE
1PRT4	PORT ONE BIT FOUR
1PRT5	PORT ONE BIT FIVE
1PRT6	PORT ONE BIT SIX
1PRT7	PORT ONE BIT SEVEN
20KHZL	20 KILOHERTZ LOW
5MHZL	5 MEGAHERTZ LOW

GLOSSARY

ac	alternating current
af	audio frequency
ant	antenna
BITE	built-in test equipment
dopp	doppler
drvr	driver
ECM	electronic countermeasures
freq	frequency
Hz	Hertz
if	intermediate frequency
intfr	interference
L.O.	local oscillator
MDS	minimum discernable signal
mon	monitor
ms	millisecond
mux	multiplexer
ovrd	overide
pa	power amplifier
prf	pulse repetition frequency
prdc	periodic
proc	processor
ps	power supply
PWM	pulse width modulator
rcvg	receiving
rcvr	radio frequency
rf	radio frequency
rfi	radio frequency interference
SCV	subclutter visibility
sw	switch
sync	synchronizer
V ac	Volts alternating current
V dc	Volts direct current
VS	volts switched
xcvr	transceiver
xmtr	transmitter
wf	waveform

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*Refer to classified supplement, TM 11-5865-201-30-2

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DATE SENT
10 July 1975

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TM 11-5840-340-12	23 Jan 74	Radar Set AN/PRC-76

E EXACT PIN-POINT WHERE IT IS

AGE NO	PARA-GRAPH	FIGURE NO	TABLE NO	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

SAMPLE

NTED NAME, GRADE OR TITLE AND TELEPHONE NUMBER	SIGN HERE
SSG I. M. DeSpiritof 999-1776	SSG I. M. DeSpiritof

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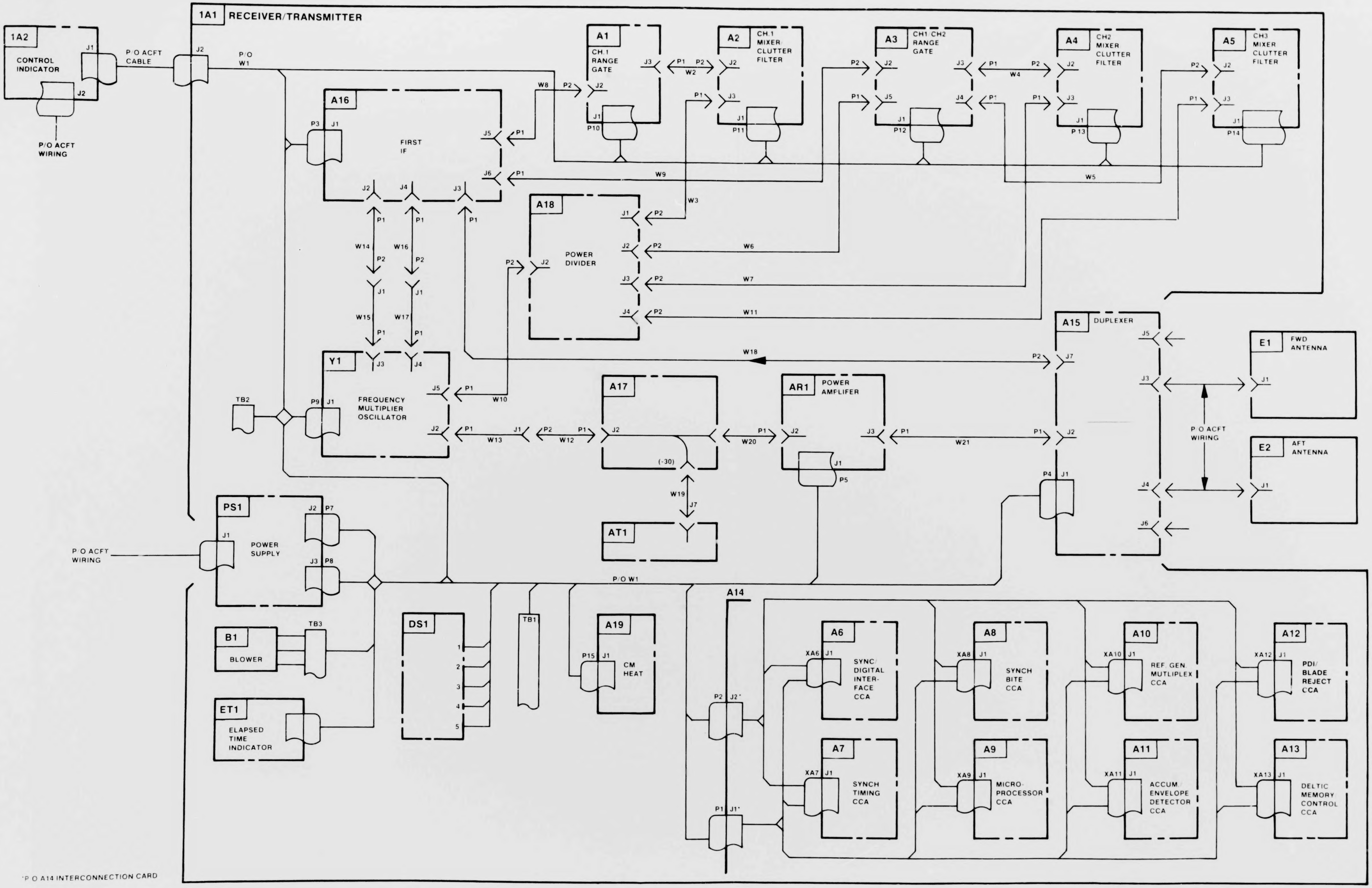
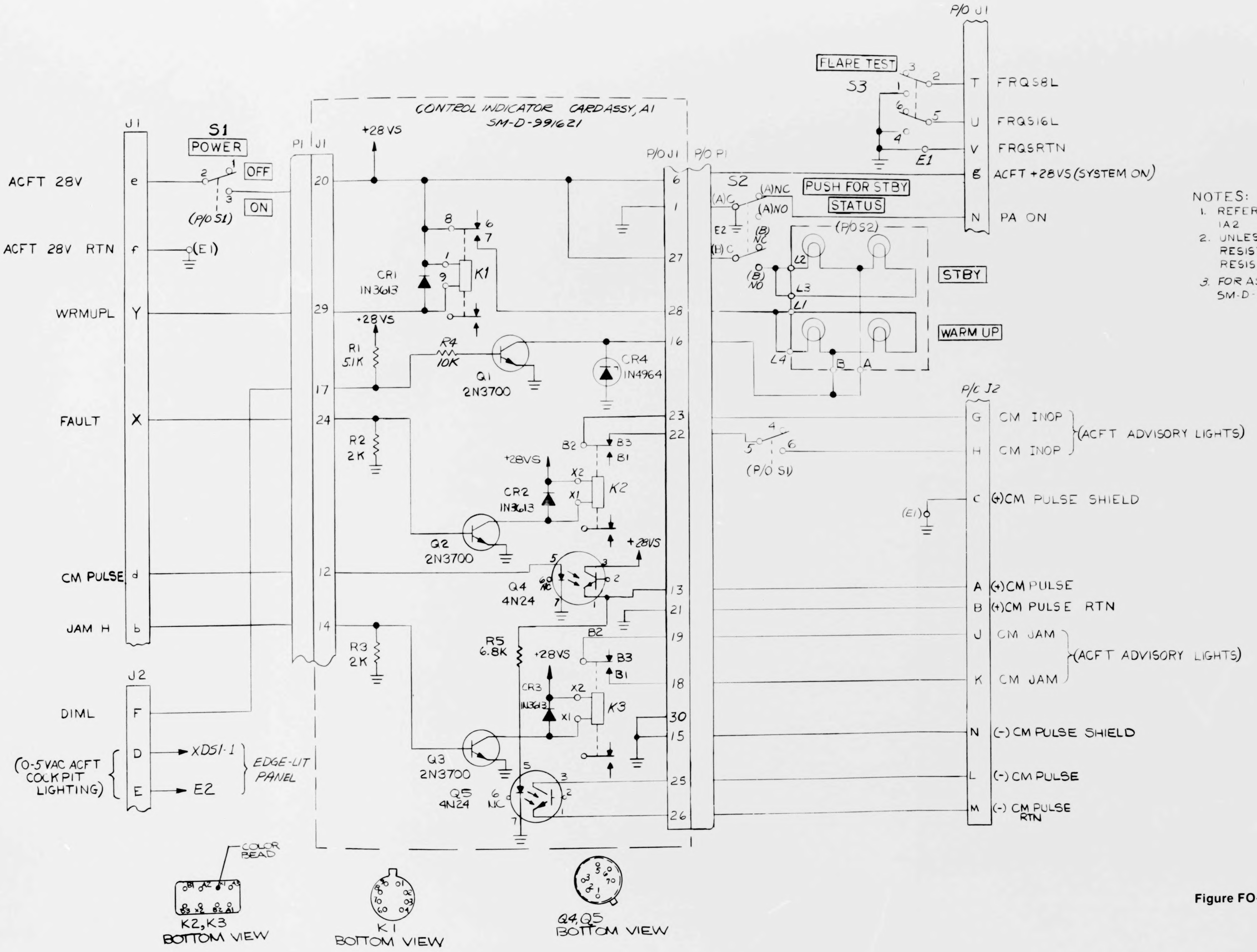

1A1 RECEIVER/TRANSMITTER
1A2
CONTROL INDICATOR
J1
J2
P/O ACFT WIRING
P/O ACFT CABLE
J2
P/O W1
A16
P3
J1
FIRST IF
J5
P1
J6
P1
J2
J4
J3
P1
P1
P1
W14
W16
P2
P2
J1
J1
W15
W17
P1
P1
Y1
J3
J4
FREQUENCY MULTIPLIER OSCILLATOR
P9
J1
J5
P1
W10
J2
P1
J1
P2
P1
W13
W12
TB2
A1
CH.1 RANGE GATE
J3
P1
P2
W2
J2
W8
P2
J1
P10
A2
CH.1 MIXER CLUTTER FILTER
J2
J3
P1
J1
P11
W3
A3
CH1 CH2 RANGE GATE
P2
J2
J3
P1
J5
J4
J1
P12
W9
A4
CH2 MIXER CLUTTER FILTER
P1
W4
P2
J2
P1
J3
J1
P13
A5
CH3 MIXER CLUTTER FILTER
P2
J2
P1
J3
J1
P14
W5
A18
POWER DIVIDER
P2
J2
J1
P2
J2
P2
W6
J3
P2
W7
J4
P2
W11
A15
DUPLEXER
J5
P2
J7
W18
J3
J1
J2
P1
P4
J1
J4
J6
E1
FWD ANTENNA
J1
P/O ACFT WIRING
E2
AFT ANTENNA
J1
A17
J2
(-30)
W19
J7
AT1
AR1
POWER AMFLIFER
P1
J2
W20
J3
P1
W21
J1
P5
PS1
POWER SUPPLY
J1
J2
P7
J3
P8
P/O ACFT WIRING
P/O W1
B1
BLOWER
TB3
ET1
ELAPSED TIME INDICATOR
DS1
1
2
3
4
5
TB1
A19
P15
J1
CM HEAT
A14
P2
J2*
P1
J1*
A6
XA6
J1
SYNC/ DIGITAL INTER-FACE CCA
A7
XA7
J1
SYNCH TIMING CCA
A8
XA8
J1
SYNCH BITE CCA
A9
XA9
J1
MICRO-PROCESSOR CCA
A10
XA10
J1
REF. GEN. MUTLIPLEX CCA
A11
XA11
J1
ACCUM ENVELOPE DETECTOR CCA
A12
XA12
J1
PDI/ BLADE REJECT CCA
A13
XA13
J1
DELTIC MEMORY CONTROL CCA
*P/O A14 INTERCONNECTION CARD

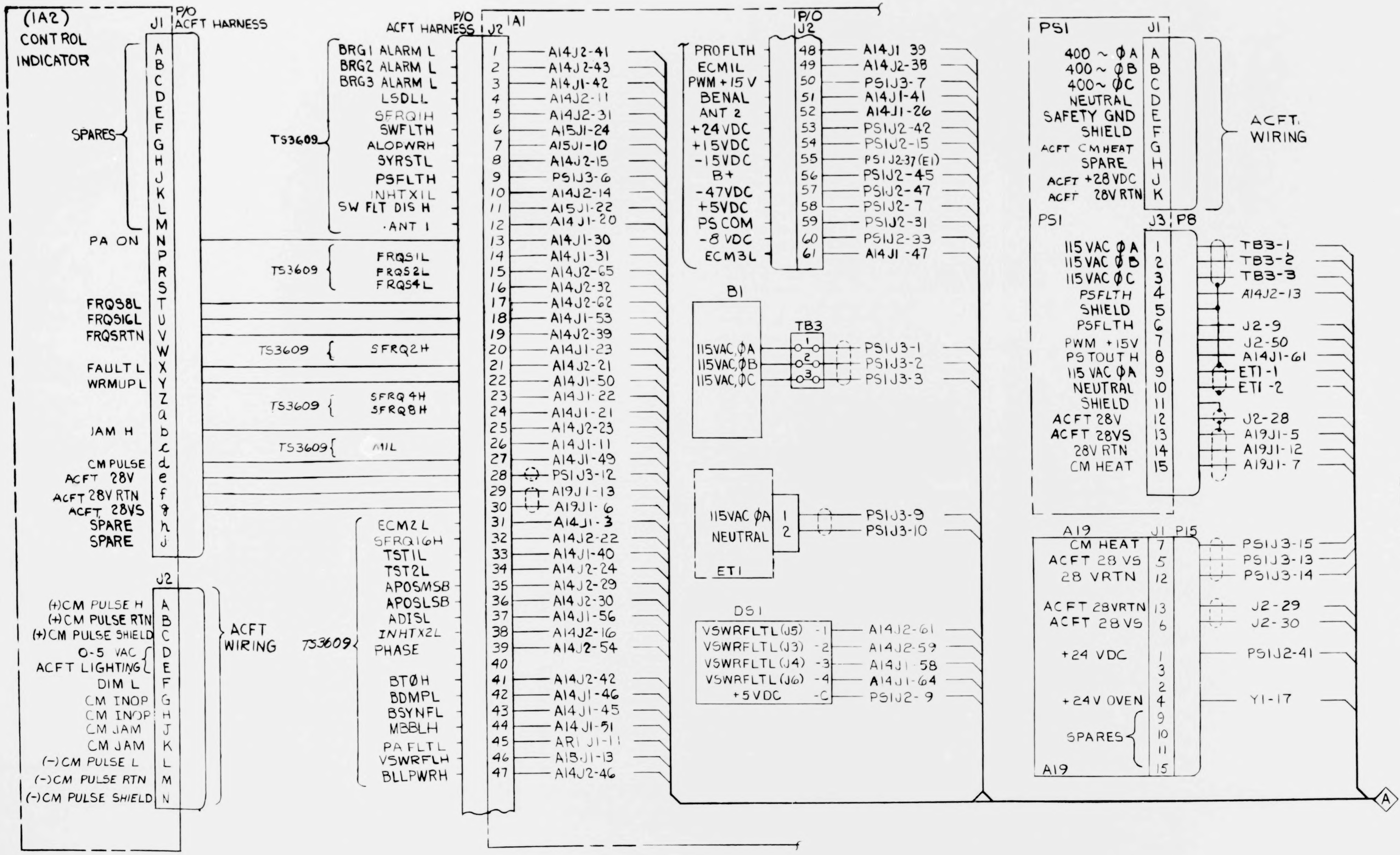
EL/E001

Figure FO-1. Countermeasures Set AN/ALQ-156(V)1 Cabling Diagram


CONTROL INDICATOR CARDASSY, A1
SM-D-991621
J1
S1
POWER
OFF
ON
(P/O S1)
ACFT 28V
ACFT 28V RTN
(E1)
WRMUPL
FAULT
CM PULSE
JAM H
J2
DIML
(0-5VAC ACFT COCKPIT LIGHTING)
XDS1-1
E2
EDGE-LIT PANEL
P1
J1
+28 VS
CR1
1N3613
K1
R1
5.1K
R4
10K
Q1
2N3700
CR4
1N4964
R2
2K
+28VS
CR2
1N3613
K2
Q2
2N3700
Q4
4N24
NC
R5
6.8K
R3
2K
CR3
1N3613
K3
Q3
2N3700
Q5
4N24
NC
P/O J1
P/O P1
S2
(A)NC
(A)NO
(A)C
E2
(B) NC
(H)C
(B) NO
PUSH FOR STBY
STATUS
(P/O S2)
L1
L2
L3
L4
STBY
WARM UP
(P/O S1)
FLARE TEST
S3
E1
P/O J1
FRQS8L
FRQS16L
FRQSRTN
ACFT +28VS (SYSTEM ON)
PA ON
P/O J2
CM INOP
CM INOP
(ACFT ADVISORY LIGHTS)
(+)CM PULSE SHIELD
(E1)
(+)CM PULSE
(+)CM PULSE RTN
CM JAM
CM JAM
(ACFT ADVISORY LIGHTS)
(-) CM PULSE SHIELD
(-) CM PULSE
(-) CM PULSE RTN
COLOR BEAD
K2,K3 BOTTOM VIEW
K1 BOTTOM VIEW
Q4,Q5 BOTTOM VIEW
EL7E00

NOTES:
1. REFERENCE DESIGNATIONS PREFIX 1A2
2. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS RESISTORS ARE ±5%, .25 W.
3. FOR ASSEMBLY SEE DWG NO SM-D-991621 & SM-D-991625

Figure FO-2. Control Indicator Interconnection Diagram


(1A2)
CONTROL INDICATOR
J1
P/O ACFT HARNESS
A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
S
T
U
V
W
X
Y
Z
a
b
c
d
e
f
g
h
j
SPARES
PA ON
FRQS8L
FRQS16L
FRQSRTN
FAULT L
WRMUP L
JAM H
CM PULSE
ACFT 28V
ACFT 28V RTN
ACFT 28VS
SPARE
SPARE
J2
(+)CM PULSE H
(+)CM PULSE RTN
(+)CM PULSE SHIELD
0-5 VAC ACFT LIGHTING
DIM L
CM INOP
CM INOP
CM JAM
CM JAM
(-)CM PULSE L
(-)CM PULSE RTN
(-)CM PULSE SHIELD
A
B
C
D
E
F
G
H
J
K
L
M
N
ACFT WIRING
P/O ACFT HARNESS
J2
1A1
TS3609
BRG1 ALARM L
BRG2 ALARM L
BRG3 ALARM L
LSDLL
SFRQ1H
SWFLTH
ALOPWRH
SYRSTL
PSFLTH
INHTX1L
SW FLT DIS H
ANT 1
TS3609
FRQS1L
FRQS2L
FRQS4L
TS3609
SFRQ2H
TS3609
SFRQ4H
SFRQ8H
TS3609
MIL
TS3609
ECM2L
SFRQ16H
TST1L
TST2L
APOSMSB
APOSLSB
ADISL
INHTX2L
PHASE
BTØH
BDMPL
BSYNFL
MBBLH
PA FLTL
VSWRFLH
BLLPWRH
1 A14J2-41
2 A14J2-43
3 A14J1-42
4 A14J2-11
5 A14J2-31
6 A15J1-24
7 A15J1-10
8 A14J2-15
9 PS1J3-6
10 A14J2-14
11 A15J1-22
12 A14J1-20
13 A14J1-30
14 A14J1-31
15 A14J2-65
16 A14J2-32
17 A14J2-62
18 A14J1-53
19 A14J2-39
20 A14J1-23
21 A14J2-21
22 A14J1-50
23 A14J1-22
24 A14J1-21
25 A14J2-23
26 A14J1-11
27 A14J1-49
28 PS1J3-12
29 A19J1-13
30 A19J1-6
31 A14J1-3
32 A14J2-22
33 A14J1-40
34 A14J2-24
35 A14J2-29
36 A14J2-30
37 A14J1-56
38 A14J2-16
39 A14J2-54
40
41 A14J2-42
42 A14J1-46
43 A14J1-45
44 A14J1-51
45 AR1 J1-11
46 A15J1-13
47 A14J2-46
P/O
J2
PROFLTH 48 A14J1 39
ECM1L 49 A14J2-38
PWM +15 V 50 PS1J3-7
BENAL 51 A14J1-41
ANT 2 52 A14J1-26
+24VDC 53 PS1J2-42
+15VDC 54 PS1J2-15
-15VDC 55 PS1J2-37(E1)
B+ 56 PS1J2-45
-47VDC 57 PS1J2-47
+5VDC 58 PS1J2-7
PS COM 59 PS1J2-31
-8 VDC 60 PS1J2-33
ECM3L 61 A14J1 -47
B1
115VAC,ØA
115VAC,ØB
115VAC,ØC
TB3
1
2
3
PS1J3-1
PS1J3-2
PS1J3-3
115VAC ØA
NEUTRAL
1
2
ET1
PS1J3-9
PS1J3-10
DS1
VSWRFLTL(J5) -1 A14J2-61
VSWRFLTL(J3) -2 A14J2-59
VSWRFLTL(J4) -3 A14J1 58
VSWRFLTL(J6) -4 A14J1-64
+5VDC -C PS1J2-9
PS1
J1
400 ~ ØA A
400 ~ ØB B
400~ ØC C
NEUTRAL D
SAFETY GND E
SHIELD F
ACFT CM HEAT G
SPARE H
ACFT +28VDC J
ACFT 28V RTN K
ACFT WIRING
PS1
J3
P8
115 VAC ØA 1 TB3-1
115 VAC ØB 2 TB3-2
115 VAC ØC 3 TB3-3
PSFLTH 4 A14J2-13
SHIELD 5
PSFLTH 6 J2-9
PWM +15V 7 J2-50
PS TOUT H 8 A14J1-61
115 VAC ØA 9 ET1-1
NEUTRAL 10 ET1-2
SHIELD 11
ACFT 28V 12 J2-28
ACFT 28VS 13 A19J1-5
28V RTN 14 A19J1-12
CM HEAT 15 A19J1-7
A19
J1
P15
CM HEAT 7 PS1J3-15
ACFT 28 VS 5 PS1J3-13
28 VRTN 12 PS1J3-14
ACFT 28VRTN 13 J2-29
ACFT 28VS 6 J2-30
+24 VDC 1 PS1J2-41
3
2
+24V OVEN 4 Y1-17
SPARES 9 10 11 15
A19
A

NOTES:

1. FOR ASSY SEE DWG NO. SM-D-991625 SM-D-920682 AND SM-A-951543.
2. FOR NON-STANDARD ABBREVIATIONS SEE DWG SM-A-920945.

EL7E003

Figure FO-3. Receiver Transmitter Interconnection Diagram (Sheet 1 of 5)

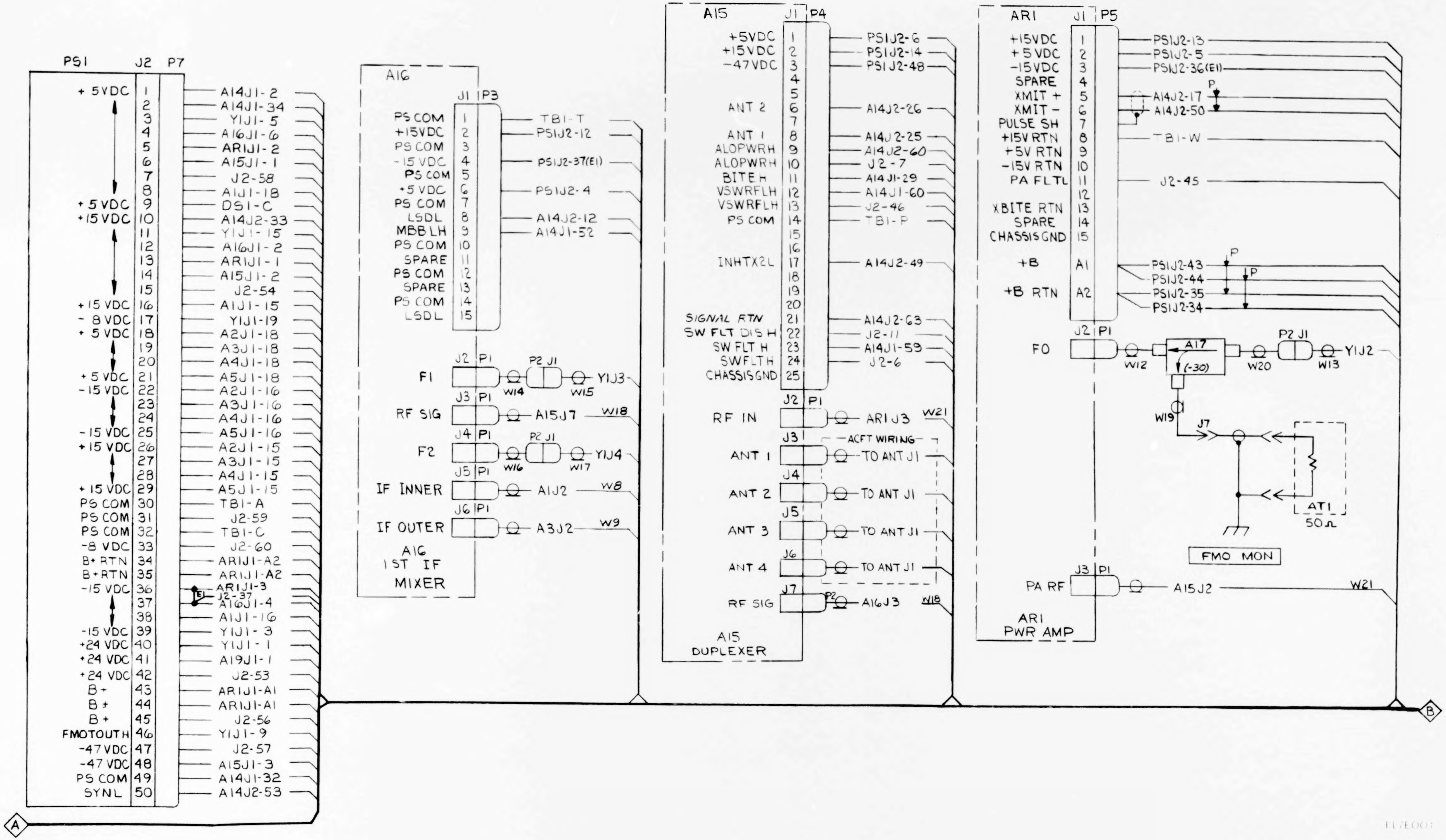

PS1
J2
P7
+ 5VDC 1 A14J1-2
2 A14J1-34
3 Y1J1-5
4 A16J1-6
5 AR1J1-2
6 A15J1-1
7 J2-58
8 A1J1-18
+ 5 VDC 9 DS1-C
+15 VDC 10 A14J2-33
11 Y1J1-15
12 A16J1-2
13 AR1J1-1
14 A15J1-2
15 J2-54
+15 VDC 16 A1J1-15
- 8 VDC 17 Y1J1-19
+ 5 VDC 18 A2J1-18
19 A3J1-18
20 A4J1-18
+ 5 VDC 21 A5J1-18
-15 VDC 22 A2J1-16
23 A3J1-16
24 A4J1-16
-15 VDC 25 A5J1-16
+15 VDC 26 A2J1-15
27 A3J1-15
28 A4J1-15
+ 15 VDC 29 A5J1-15
PS COM 30 TB1-A
PS COM 31 J2-59
PS COM 32 TB1-C
-8 VDC 33 J2-60
B+ RTN 34 AR1J1-A2
B+ RTN 35 AR1J1-A2
-15 VDC 36 AR1J1-3
E1 J2-37
37 A16J1-4
38 A1J1-16
-15 VDC 39 Y1J1-3
+24 VDC 40 Y1J1-1
+24 VDC 41 A19J1-1
+24 VDC 42 J2-53
B+ 43 AR1J1-A1
B+ 44 AR1J1-A1
B+ 45 J2-56
FMOTOUTH 46 Y1J1-9
-47 VDC 47 J2-57
-47 VDC 48 A15J1-3
PS COM 49 A14J1-32
SYNL 50 A14J2-53
A
A16
J1 P3
PS COM 1 TB1-T
+15VDC 2 PS1J2-12
PS COM 3
-15 VDC 4 PS1J2-37(E1)
PS COM 5
+5 VDC 6 PS1J2-4
PS COM 7
LSDL 8 A14J2-12
MBBLH 9 A14J1-52
PS COM 10
SPARE 11
PS COM 12
SPARE 13
PS COM 14
LSDL 15
J2 P1 F1 W14 P2 J1 W15 Y1J3
J3 P1 RF SIG A15J7 W18
J4 P1 F2 W16 P2 J1 W17 Y1J4
J5 P1 IF INNER A1J2 W8
J6 P1 IF OUTER A3J2 W9
A16
1ST IF
MIXER
A15
J1 P4
+5VDC 1 PS1J2-6
+15VDC 2 PS1J2-14
-47VDC 3 PS1J2-48
4
5
ANT 2 6 A14J2-26
7
ANT 1 8 A14J2-25
ALOPWRH 9 A14J2-60
ALOPWRH 10 J2-7
BITE H 11 A14J1-29
VSWRFLH 12 A14J1-60
VSWRFLH 13 J2-46
PS COM 14 TB1-P
15
16
INHTX2L 17 A14J2-49
18
19
20
SIGNAL RTN 21 A14J2-63
SW FLT DIS H 22 J2-11
SW FLT H 23 A14J1-59
SWFLTH 24 J2-6
CHASSIS GND 25
J2 P1 RF IN AR1J3 W21
J3 ANT 1 TO ANT J1
ACFT WIRING
J4 ANT 2 TO ANT J1
J5 ANT 3 TO ANT J1
J6 ANT 4 TO ANT J1
J7 P2 RF SIG A16J3 W18
A15
DUPLEXER
AR1
J1 P5
+15VDC 1 PS1J2-13
+5 VDC 2 PS1J2-5
-15VDC 3 PS1J2-36(E1)
SPARE 4
XMIT + 5 A14J2-17
XMIT - 6 A14J2-50
P
PULSE SH 7
+15V RTN 8 TB1-W
+5V RTN 9
-15V RTN 10
PA FLTL 11 J2-45
12
XBITE RTN 13
SPARE 14
CHASSIS GND 15
+B A1 PS1J2-43
PS1J2-44
+B RTN A2 PS1J2-35
PS1J2-34
P
J2 P1 FO W12 A17 (-30) W20 P2 J1 W13 Y1J2
W19 J7
AT1 50Ω
FMO MON
J3 P1 PA RF A15J2 W21
AR1
PWR AMP
B

Figure FO-3. Receiver Transmitter Interconnection Diagram (Sheet 2 of 5)

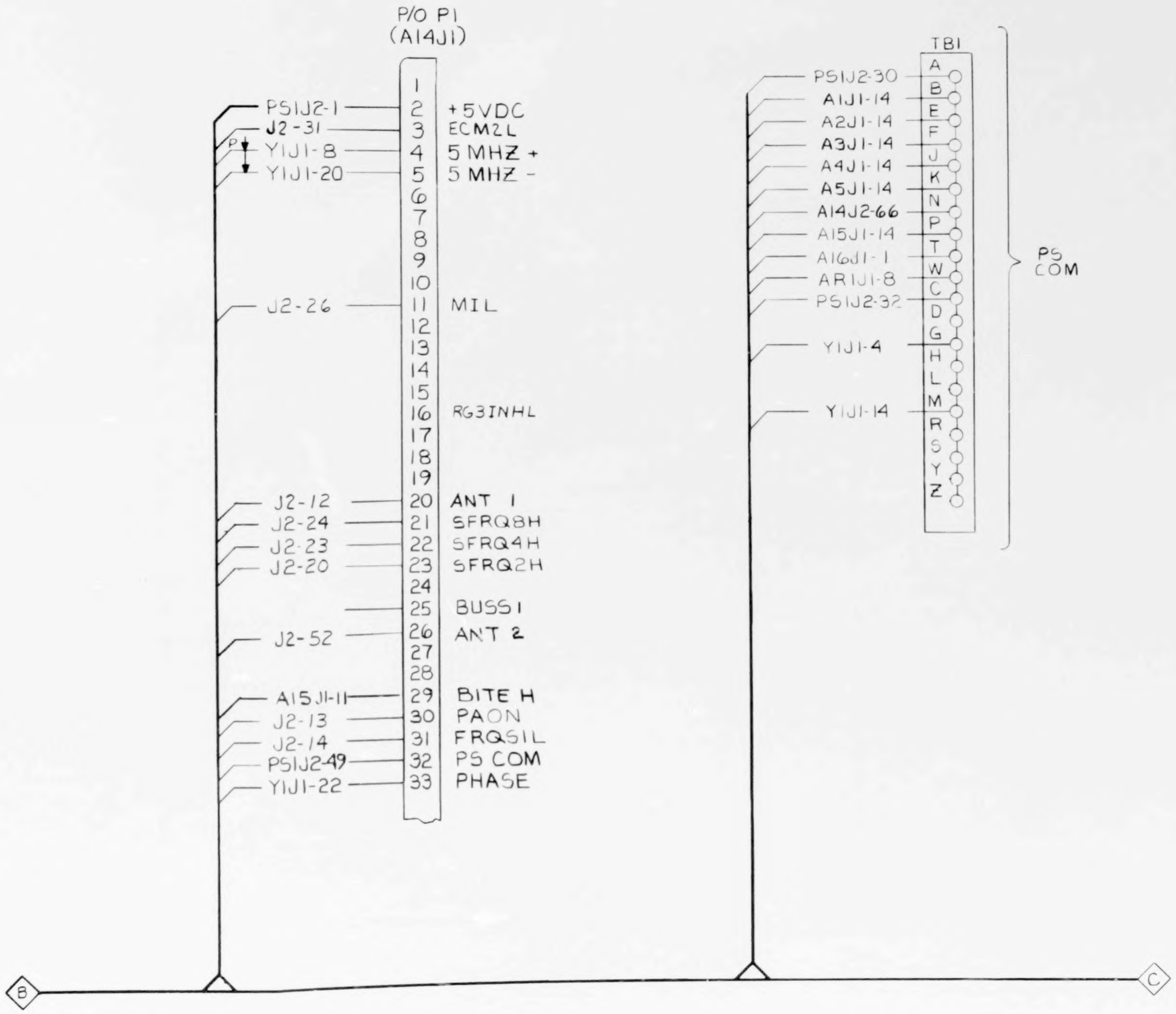
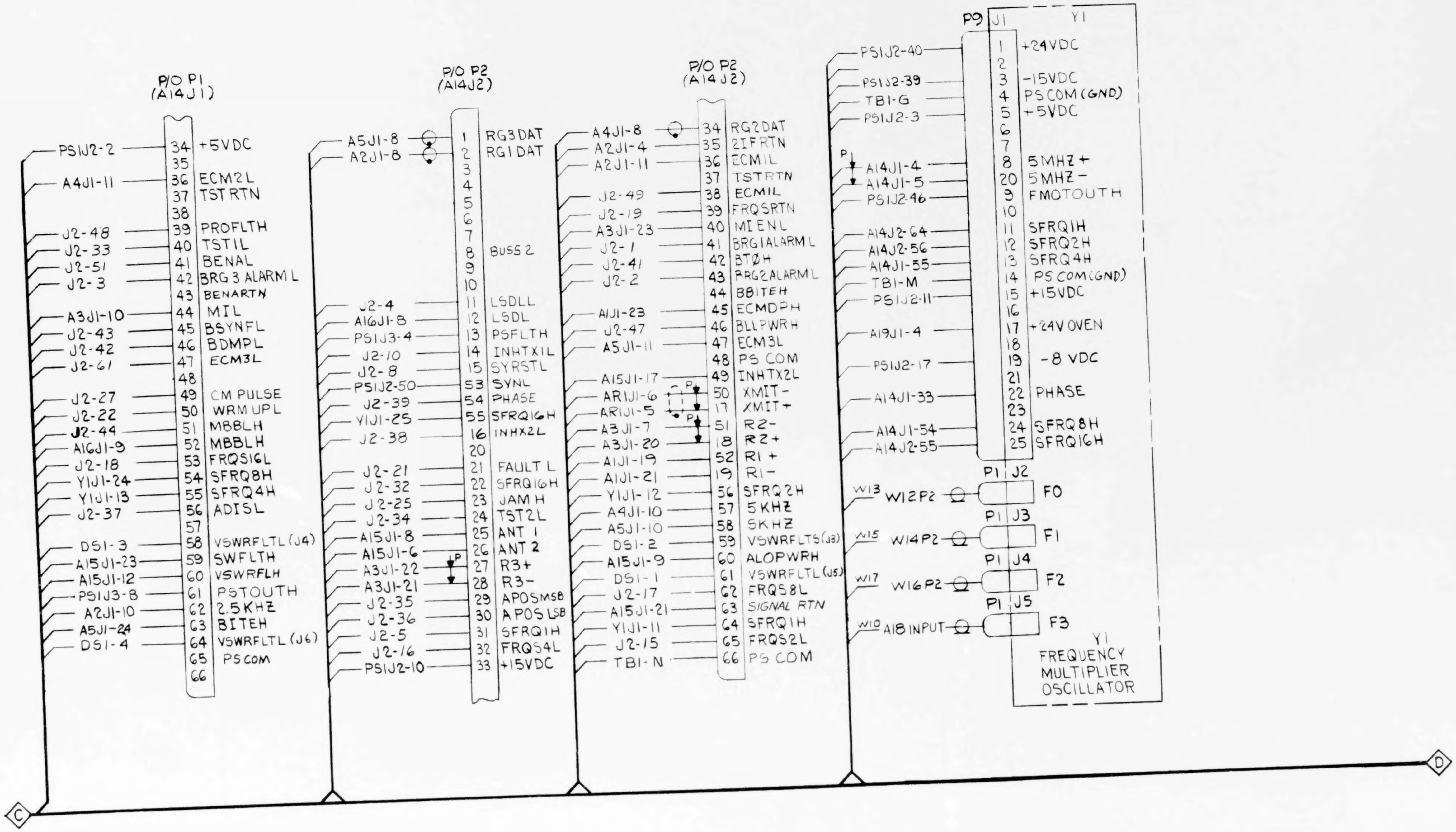

P/O P1
(A14J1)
1
PS1J2-1 2 +5VDC
J2-31 3 ECM2L
P
Y1J1-8 4 5 MHZ +
Y1J1-20 5 5 MHZ -
6
7
8
9
10
J2-26 11 MIL
12
13
14
15
16 RG3INHL
17
18
19
J2-12 20 ANT 1
J2-24 21 SFRQ8H
J2-23 22 SFRQ4H
J2-20 23 SFRQ2H
24
25 BUSS1
J2-52 26 ANT 2
27
28
A15J1-11 29 BITE H
J2-13 30 PAON
J2-14 31 FRQSIL
PS1J2-49 32 PS COM
Y1J1-22 33 PHASE
TB1
PS1J2-30 A
A1J1-14 B
A2J1-14 E
A3J1-14 F
A4J1-14 J
A5J1-14 K
A14J2-66 N
A15J1-14 P
A16J1-1 T
AR1J1-8 W
PS1J2-32 C
D
Y1J1-4 G
H
L
Y1J1-14 M
R
S
Y
Z
PS
COM
B
C

Figure FO-3. Receiver Transmitter Interconnection Diagram (Sheet 3 of 5)


P/O P1
(A14J1)
PS1J2-2 34 +5VDC
35
A4J1-11 36 ECM2L
37 TST RTN
38
J2-48 39 PROFLTH
J2-33 40 TSTIL
J2-51 41 BENAL
J2-3 42 BRG 3 ALARM L
43 BENARTN
A3J1-10 44 MIL
J2-43 45 BSYNFL
J2-42 46 BDMPL
J2-61 47 ECM3L
48
J2-27 49 CM PULSE
J2-22 50 WRM UPL
J2-44 51 MBBLH
A16J1-9 52 MBBLH
J2-18 53 FRQS16L
Y1J1-24 54 SFRQ8H
Y1J1-13 55 SFRQ4H
J2-37 56 ADISL
57
DS1-3 58 VSWRFLTL (J4)
A15J1-23 59 SWFLTH
A15J1-12 60 VSWRFLH
PS1J3-8 61 PSTOUTH
A2J1-10 62 2.5KHZ
A5J1-24 63 BITEH
DS1-4 64 VSWRFLTL (J6)
65 PS COM
66
P/O P2
(A14J2)
A5J1-8 1 RG3DAT
A2J1-8 2 RG1DAT
3
4
5
6
7
8 BUSS 2
9
10
J2-4 11 LSDLL
A16J1-8 12 LSDL
PS1J3-4 13 PSFLTH
J2-10 14 INHTX1L
J2-8 15 SYRSTL
PS1J2-50 53 SYNL
J2-39 54 PHASE
Y1J1-25 55 SFRQ16H
J2-38 16 INHX2L
20
J2-21 21 FAULT L
J2-32 22 SFRQ16H
J2-25 23 JAM H
J2-34 24 TST2L
A15J1-8 25 ANT 1
A15J1-6 26 ANT 2
P
A3J1-22 27 R3+
A3J1-21 28 R3-
J2-35 29 APOS MSB
J2-36 30 APOS LSB
J2-5 31 SFRQ1H
J2-16 32 FRQS4L
PS1J2-10 33 +15VDC
P/O P2
(A14J2)
A4J1-8 34 RG2DAT
A2J1-4 35 2IFRTN
A2J1-11 36 ECM1L
37 TSTRTN
J2-49 38 ECMIL
J2-19 39 FRQSRTN
A3J1-23 40 MIENL
J2-1 41 BRG1ALARM L
J2-41 42 BTØH
J2-2 43 BRG2ALARM L
44 BBITEH
A1J1-23 45 ECMDPH
J2-47 46 BLLPWRH
A5J1-11 47 ECM3L
48 PS COM
A15J1-17 49 INHTX2L
P
AR1J1-6 50 XMIT-
AR1J1-5 17 XMIT+
P
A3J1-7 51 R2-
A3J1-20 18 R2+
A1J1-19 52 R1 +
A1J1-21 19 R1-
Y1J1-12 56 SFRQ2H
A4J1-10 57 5KHZ
A5J1-10 58 5KHZ
DS1-2 59 VSWRFLTS(J3)
A15J1-9 60 ALOPWRH
DS1-1 61 VSWRFLTL(J5)
J2-17 62 FRQS8L
A15J1-21 63 SIGNAL RTN
Y1J1-11 64 SFRQ1H
J2-15 65 FRQS2L
TB1-N 66 PS COM
P9 J1 Y1
PS1J2-40 1 +24VDC
2
PS1J2-39 3 -15VDC
TB1-G 4 PS COM (GND)
PS1J2-3 5 +5VDC
6
7
P
A14J1-4 8 5MHZ+
A14J1-5 20 5MHZ-
PS1J2-46 9 FMOTOUTH
10
A14J2-64 11 SFRQ1H
A14J2-56 12 SFRQ2H
A14J1-55 13 SFRQ4H
TB1-M 14 PS COM (GND)
PS1J2-11 15 +15VDC
16
A19J1-4 17 +24V OVEN
18
PS1J2-17 19 -8 VDC
21
A14J1-33 22 PHASE
23
A14J1-54 24 SFRQ8H
A14J2-55 25 SFRQ16H
P1 J2
W13 W12P2 F0
P1 J3
W15 W14P2 F1
P1 J4
W17 W16P2 F2
P1 J5
W10 A18 INPUT F3
Y1
FREQUENCY
MULTIPLIER
OSCILLATOR
C
D

EL7C006

Figure FO-3. Receiver Transmitter Interconnection Diagram (Sheet 4 of 5)

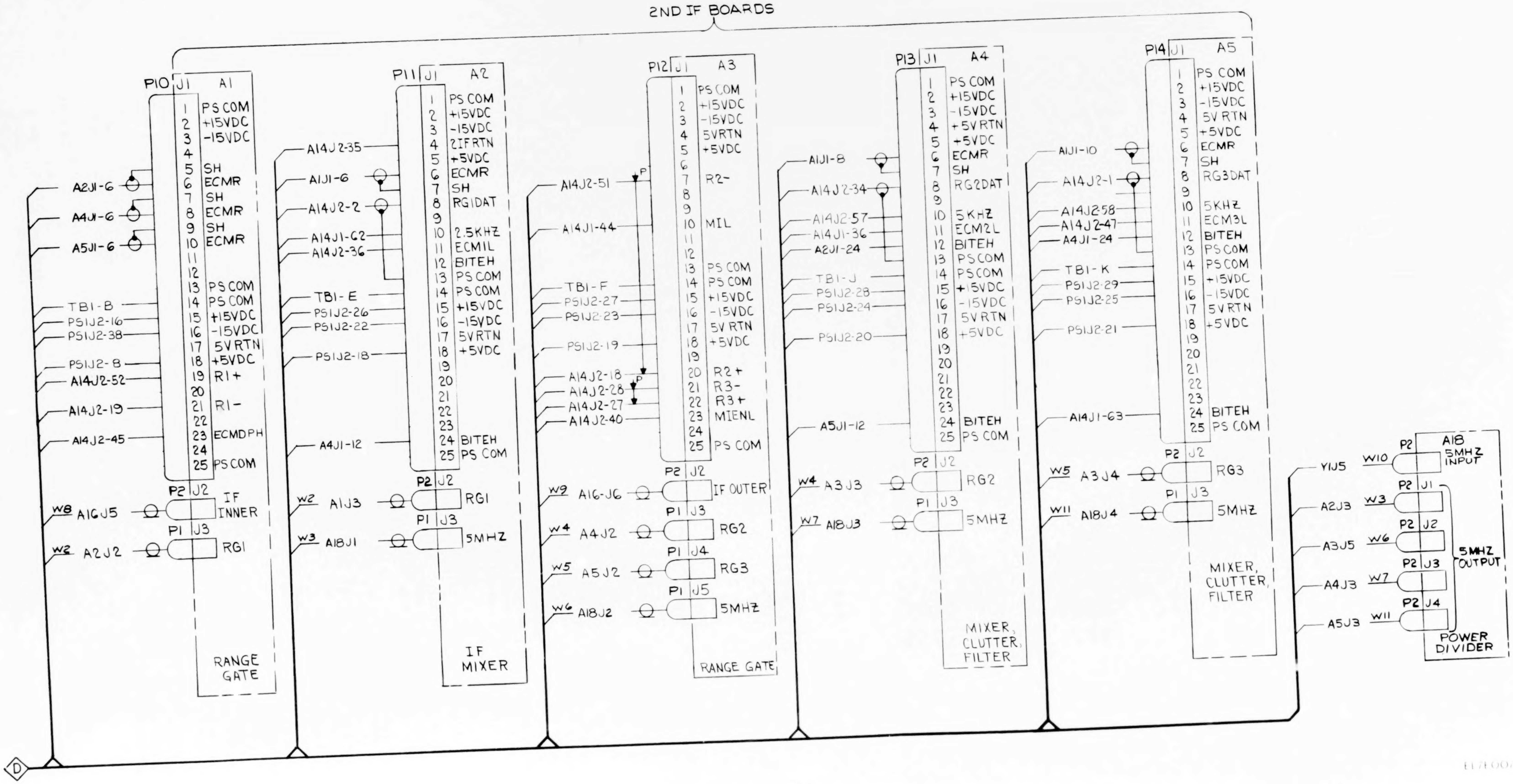
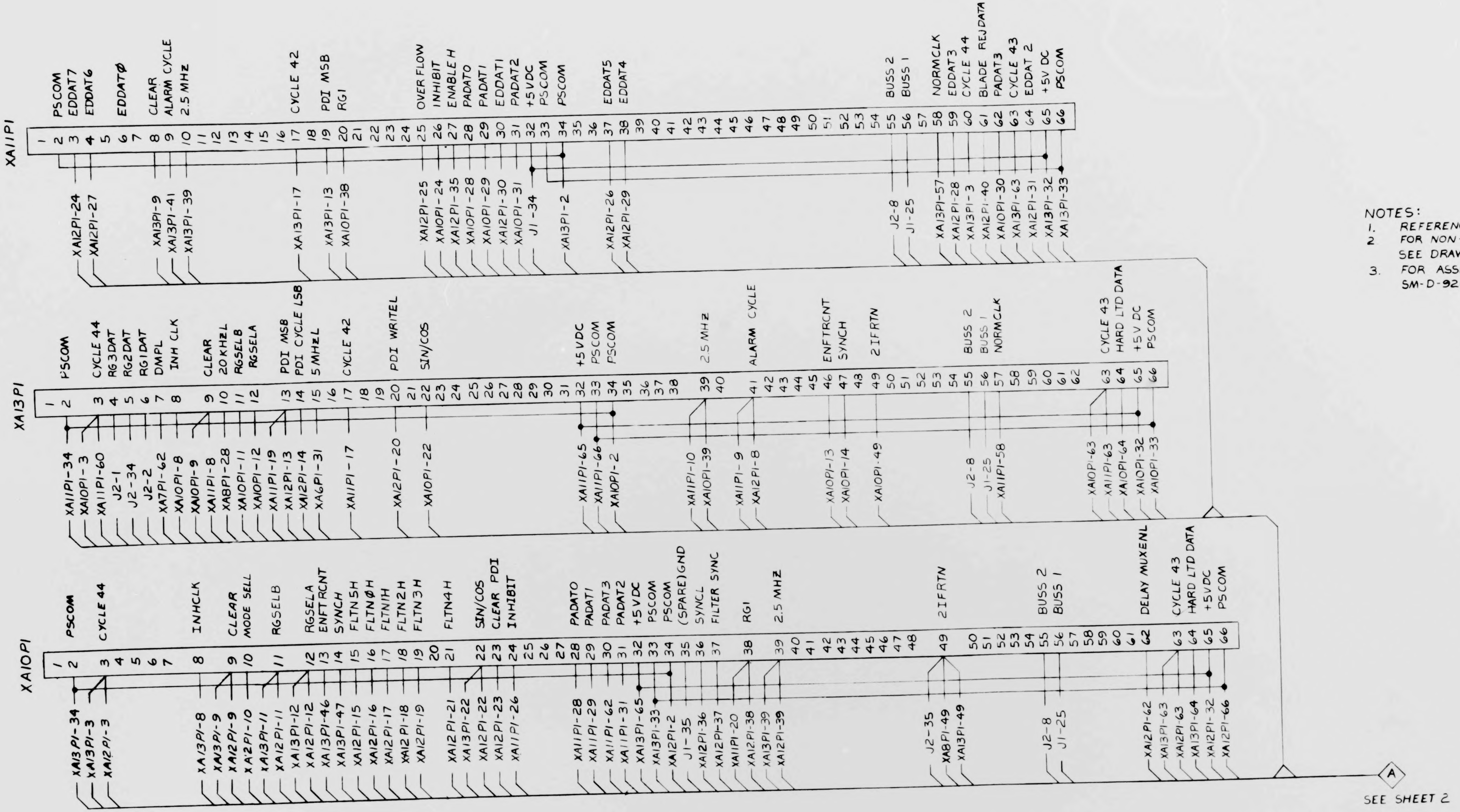

2ND IF BOARDS
P10 J1 A1
1 PS COM
2 +15VDC
3 -15VDC
4
5 SH
6 ECMR
7 SH
8 ECMR
9 SH
10 ECMR
11
12
13 PS COM
14 PS COM
15 +15VDC
16 -15VDC
17 5VRTN
18 +5VDC
19 R1+
20
21 R1-
22
23 ECMDPH
24
25 PS COM
A2J1-6
A4J1-6
A5J1-6
TB1-B
PS1J2-16
PS1J2-38
PS1J2-8
A14J2-52
A14J2-19
A14J2-45
P2 J2 IF INNER
W8 A16J5
P1 J3 RG1
W2 A2J2
RANGE GATE
P11 J1 A2
1 PS COM
2 +15VDC
3 -15VDC
4 2IFRTN
5 +5VDC
6 ECMR
7 SH
8 RG1DAT
9
10 2.5KHZ
11 ECM1L
12 BITEH
13 PS COM
14 PS COM
15 +15VDC
16 -15VDC
17 5VRTN
18 +5VDC
19
20
21
22
23
24 BITEH
25 PS COM
A14J2-35
A1J1-6
A14J2-2
A14J1-62
A14J2-36
TB1-E
PS1J2-26
PS1J2-22
PS1J2-18
A4J1-12
P2 J2 RG1
W2 A1J3
P1 J3 5MHZ
W3 A18J1
IF MIXER
P12 J1 A3
1 PS COM
2 +15VDC
3 -15VDC
4 5VRTN
5 +5VDC
6
7 R2-
8
9
10 MIL
11
12
13 PS COM
14 PS COM
15 +15VDC
16 -15VDC
17 5V RTN
18 +5VDC
19
20 R2+
21 R3-
22 R3+
23 MIENL
24
25 PS COM
A14J2-51
A14J1-44
TB1-F
PS1J2-27
PS1J2-23
PS1J2-19
A14J2-18
A14J2-28
A14J2-27
A14J2-40
P
P
P2 J2 IF OUTER
W9 A16-J6
P1 J3 RG2
W4 A4J2
P1 J4 RG3
W5 A5J2
P1 J5 5MHZ
W6 A18J2
RANGE GATE
P13 J1 A4
1 PS COM
2 +15VDC
3 -15VDC
4 +5VRTN
5 +5VDC
6 ECMR
7 SH
8 RG2DAT
9
10 5KHZ
11 ECM2L
12 BITEH
13 PS COM
14 PS COM
15 +15VDC
16 -15VDC
17 5VRTN
18 +5VDC
19
20
21
22
23
24 BITEH
25 PS COM
A1J1-8
A14J2-34
A14J2-57
A14J1-36
A2J1-24
TB1-J
PS1J2-28
PS1J2-24
PS1J2-20
A5J1-12
P2 J2 RG2
W4 A3J3
P1 J3 5MHZ
W7 A18J3
MIXER, CLUTTER, FILTER
P14 J1 A5
1 PS COM
2 +15VDC
3 -15VDC
4 5V RTN
5 +5VDC
6 ECMR
7 SH
8 RG3DAT
9
10 5KHZ
11 ECM3L
12 BITEH
13 PS COM
14 PS COM
15 +15VDC
16 -15VDC
17 5VRTN
18 +5VDC
19
20
21
22
23
24 BITEH
25 PS COM
A1J1-10
A14J2-1
A14J2-58
A14J2-47
A4J1-24
TB1-K
PS1J2-29
PS1J2-25
PS1J2-21
A14J1-63
P2 J2 RG3
W5 A3J4
P1 J3 5MHZ
W11 A18J4
MIXER, CLUTTER, FILTER
P2 A18 5MHZ INPUT
Y1J5 W10
P2 J1
A2J3 W3
P2 J2
A3J5 W6
P2 J3
A4J3 W7
P2 J4
A5J3 W11
5MHZ OUTPUT
POWER DIVIDER
D

Figure FO-3. Receiver Transmitter Interconnection Diagram (Sheet 5 of 5)


XA11P1
XA13P1
XA10P1
A
SEE SHEET 2

NOTES:
1. REFERENCE DESIGNATION PREFIX 1A1
2. FOR NON-STANDARD ABBREVIATIONS SEE DRAWING SM-D-920945.
3. FOR ASSEMBLY DRAWING SEE SM-D-920761.

Figure FO-4. Circuit Card Assembly A14 Connection Diagram (Sheet 1 of 4)

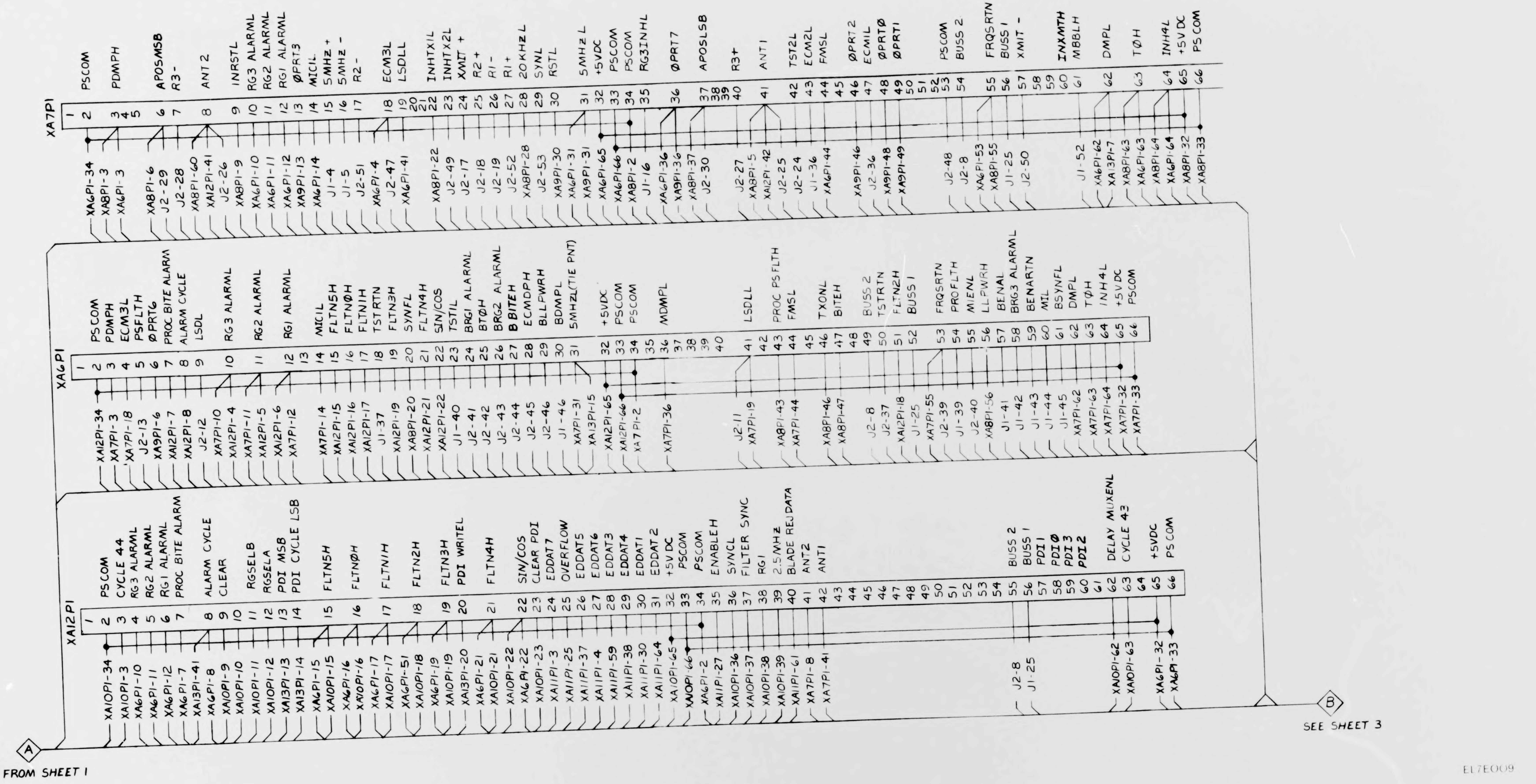

XA7P1
XA6P1
XA12P1
A
FROM SHEET 1
B
SEE SHEET 3
EL7EO09

Figure FO-4. Circuit Card Assembly A14 Connection Diagram (Sheet 2 of 4)

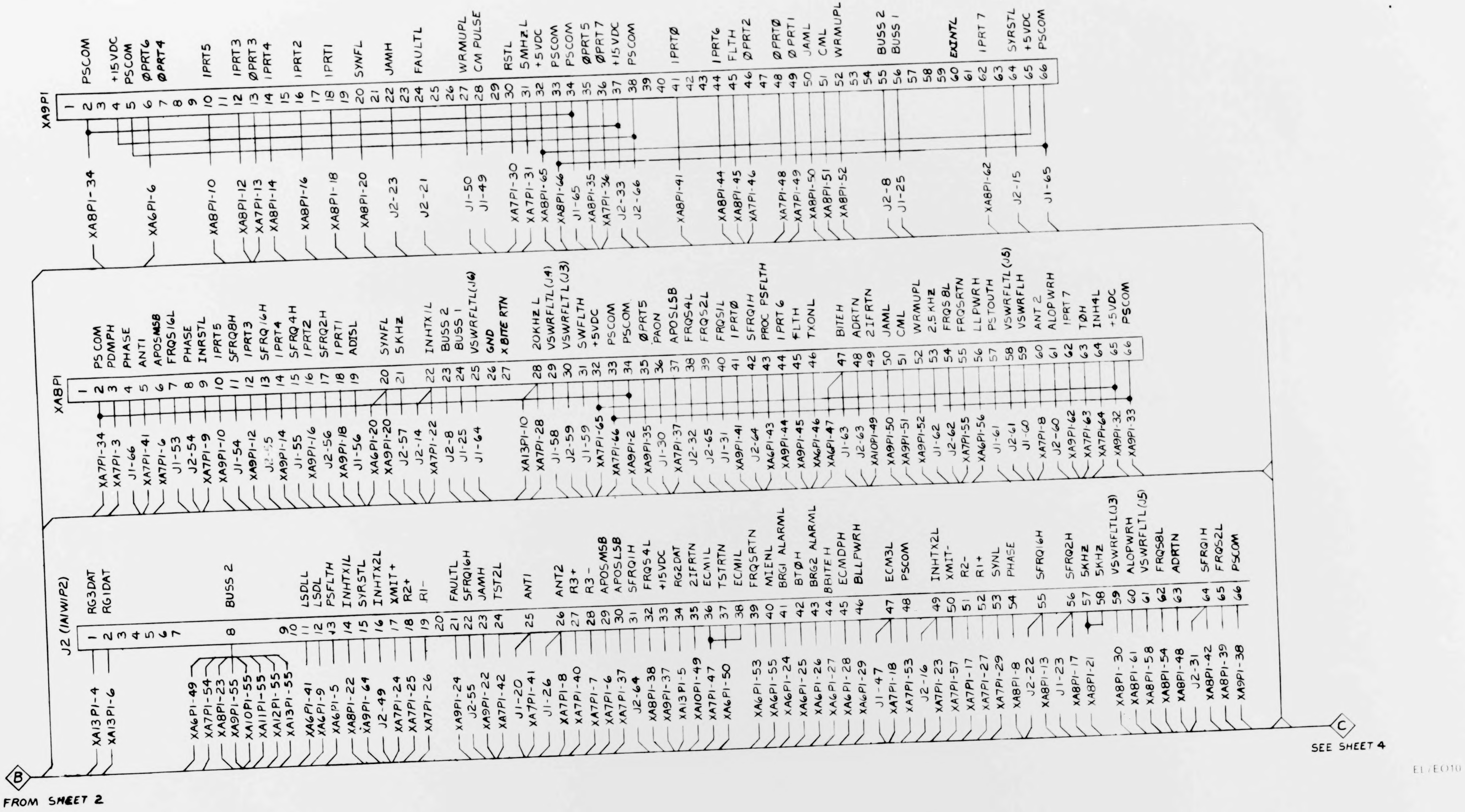
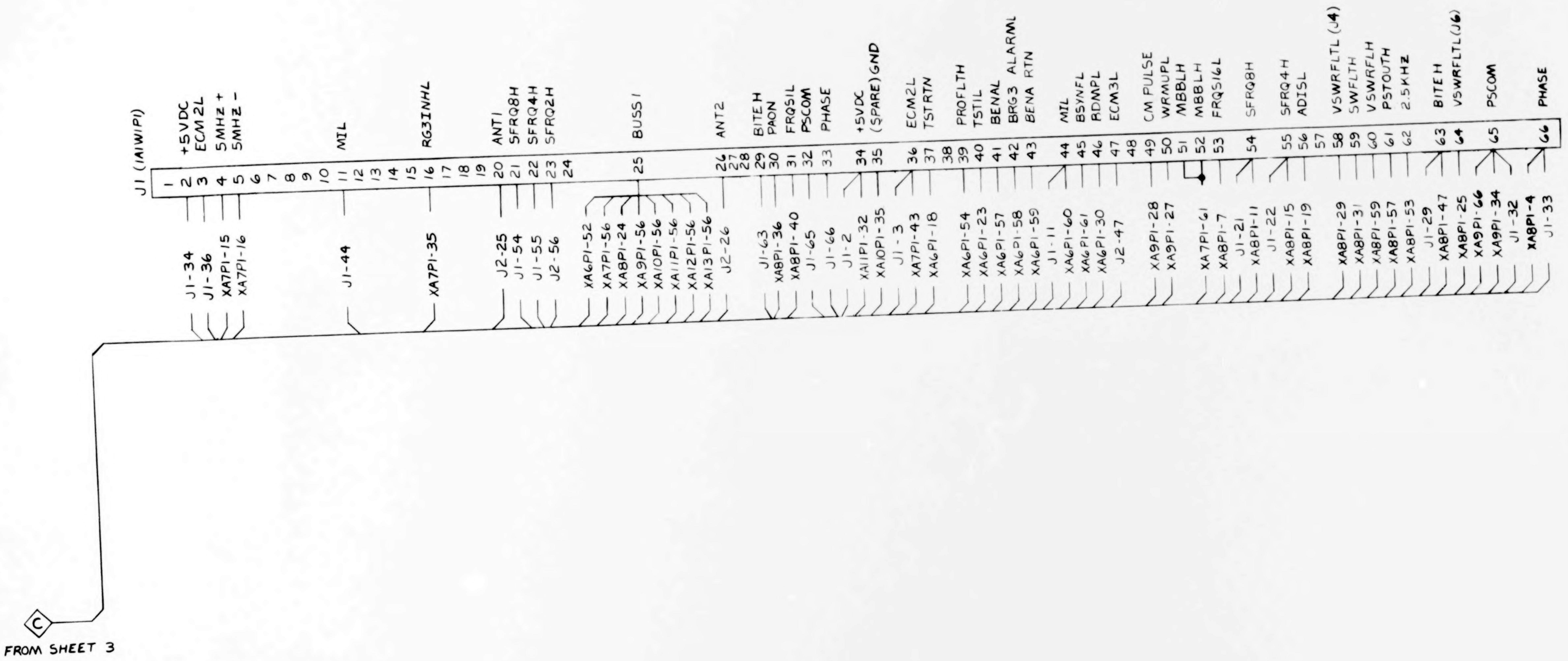

XA9P1
PSCOM
+15VDC
PSCOM
ØPRT6
ØPRT4
IPRT5
IPRT3
ØPRT3
IPRT4
IPRT2
IPRT1
SYNFL
JAMH
FAULTL
WRMUPL
CM PULSE
RSTL
5MHZ L
+5VDC
PSCOM
PSCOM
ØPRT5
ØPRT7
+15VDC
PSCOM
IPRTØ
IPRT6
FLTH
ØPRT2
ØPRTØ
ØPRT1
JAML
CML
WRMUPL
BUSS 2
BUSS 1
EXINTL
IPRT 7
SYRSTL
+5VDC
PSCOM
XA8P1-34
XA6P1-6
XA8P1-10
XA8P1-12
XA7P1-13
XA8P1-14
XA8P1-16
XA8P1-18
XA8P1-20
J2-23
J2-21
J1-50
J1-49
XA7P1-30
XA7P1-31
XA8P1-65
XA8P1-66
J1-65
XA8P1-35
XA7P1-36
J2-33
J2-66
XA8P1-41
XA8P1-44
XA8P1-45
XA7P1-46
XA7P1-48
XA7P1-49
XA8P1-50
XA8P1-51
XA8P1-52
J2-8
J1-25
XA8P1-62
J2-15
J1-65
XA8P1
PSCOM
PDMPH
PHASE
ANT1
APOSMSB
FRQS16L
PHASE
INRSTL
IPRT5
SFRQ8H
IPRT3
SFRQ16H
IPRT4
SFRQ4H
IPRT2
SFRQ2H
IPRT1
ADISL
SYNFL
5KHZ
INHTX1L
BUSS 2
BUSS 1
VSWRFLTL(J6)
GND
X BITE RTN
20KHZ L
VSWRFLTL(J4)
VSWRFLTL(J3)
SWFLTH
+5VDC
PSCOM
PSCOM
ØPRT5
PAON
APOSLSB
FRQS4L
FRQS2L
FRQS1L
IPRTØ
SFRQ1H
PROC PSFLTH
IPRT6
FLTH
TXONL
BITEH
ADRTN
2IFRTN
JAML
CML
WRMUPL
2.5KHZ
FRQS8L
FRQSRTN
LLPWRH
PSTOUTH
VSWRFLTL(J5)
VSWRFLH
ANT 2
ALOPWRH
IPRT7
TØH
INH4L
+5VDC
PSCOM
XA7P1-34
XA7P1-3
J1-66
XA7P1-41
XA7P1-6
J1-53
J2-54
XA7P1-9
XA9P1-10
J1-54
XA9P1-12
J2-55
XA9P1-14
J1-55
XA9P1-16
J2-56
XA9P1-18
J1-56
XA6P1-20
XA9P1-20
J2-57
J2-14
XA7P1-22
J2-8
J1-25
J1-64
XA13P1-10
XA7P1-28
J1-58
J2-59
J1-59
XA7P1-65
XA7P1-66
XA9P1-2
XA9P1-35
J1-30
XA7P1-37
J2-32
J2-65
J1-31
XA9P1-41
J2-64
XA6P1-43
XA9P1-44
XA9P1-45
XA6P1-46
XA6P1-47
J1-63
J2-63
XA10P1-49
XA9P1-50
XA9P1-51
XA9P1-52
J1-62
J2-62
XA7P1-55
XA6P1-56
J1-61
J2-61
J1-60
XA7P1-8
J2-60
XA9P1-62
XA7P1-63
XA7P1-64
XA9P1-32
XA9P1-33
J2 (1A1W1P2)
RG3DAT
RG1DAT
BUSS 2
LSDLL
LSDL
PSFLTH
INHTX1L
SYRSTL
INHTX2L
XMIT+
R2+
R1-
FAULTL
SFRQ16H
JAMH
TST2L
ANT1
ANT2
R3+
R3-
APOSMSB
APOSLSB
SFRQ1H
FRQS4L
+15VDC
RG2DAT
2IFRTN
ECM1L
TSTRTN
ECMIL
FRQSRTN
MIENL
BRG1 ALARML
BTØH
BRG2 ALARML
BRITE H
ECMDPH
BLLPWRH
ECM3L
PSCOM
INHTX2L
XMIT-
R2-
R1+
SYNL
PHASE
SFRQ16H
SFRQ2H
5KHZ
5KHZ
VSWRFLTL(J3)
ALOPWRH
VSWRFLTL(J5)
FRQS8L
ADRTN
SFRQ1H
FRQS2L
PSCOM
XA13P1-4
XA13P1-6
XA6P1-49
XA7P1-54
XA8P1-23
XA9P1-55
XA10P1-55
XA11P1-55
XA12P1-55
XA13P1-55
XA6P1-41
XA6P1-9
XA6P1-5
XA8P1-22
XA9P1-64
J2-49
XA7P1-24
XA7P1-25
XA7P1-26
XA9P1-24
J2-55
XA9P1-22
XA7P1-42
J1-20
XA7P1-41
J1-26
XA7P1-8
XA7P1-40
XA7P1-7
XA7P1-6
XA7P1-37
J2-64
XA8P1-38
XA9P1-37
XA13P1-5
XA10P1-49
XA7P1-47
XA6P1-50
XA6P1-53
XA6P1-55
XA6P1-24
XA6P1-25
XA6P1-26
XA6P1-27
XA6P1-28
XA6P1-29
J1-47
XA7P1-18
XA7P1-53
J2-16
XA7P1-23
XA7P1-57
XA7P1-17
XA7P1-27
XA7P1-29
XA8P1-8
J2-22
XA8P1-13
J1-23
XA8P1-17
XA8P1-21
XA8P1-30
XA8P1-61
XA8P1-58
XA8P1-54
XA8P1-48
J2-31
XA8P1-42
XA8P1-39
XA9P1-38
B
FROM SHEET 2
C
SEE SHEET 4
EL/EO10

Figure FO-4. Circuit Card Assembly A14 Connection Diagram (Sheet 3 of 4)


J1 (1A1W1P1)
1
2 +5VDC
3 ECM2L
4 5MHz +
5 5MHz -
6
7
8
9
10
11 MIL
12
13
14
15
16 RG3INHL
17
18
19
20 ANT1
21 SFRQ8H
22 SFRQ4H
23 SFRQ2H
24
25 BUSS1
26 ANT2
27
28
29 BITE H
30 PAON
31 FRQSIL
32 PSCOM
33 PHASE
34 +5VDC
35 (SPARE) GND
36 ECM2L
37 TSTRTN
38
39 PROFLTH
40 TSTIL
41 BENAL
42 BRG3 ALARML
43 BENA RTN
44 MIL
45 BSYNFL
46 RDMPL
47 ECM3L
48
49 CM PULSE
50 WRMUPL
51 MBBLH
52 MBBLH
53 FRQSI6L
54 SFRQ8H
55 SFRQ4H
56 ADISL
57
58 VSWRFLTL (J4)
59 SWFLTH
60 VSWRFLH
61 PSTOUTH
62 2.5KHZ
63 BITE H
64 VSWRFLTL (J6)
65 PSCOM
66 PHASE
J1-34
J1-36
XA7P1-15
XA7P1-16
J1-44
XA7P1-35
J2-25
J1-54
J1-55
J2-56
XA6P1-52
XA7P1-56
XA8P1-24
XA9P1-56
XA10P1-56
XA11P1-56
XA12P1-56
XA13P1-56
J2-26
J1-63
XA8P1-36
XA8P1-40
J1-65
J1-66
J1-2
XA11P1-32
XA10P1-35
J1-3
XA7P1-43
XA6P1-18
XA6P1-54
XA6P1-23
XA6P1-57
XA6P1-58
XA6P1-59
J1-11
XA6P1-60
XA6P1-61
XA6P1-30
J2-47
XA9P1-28
XA9P1-27
XA7P1-61
XA8P1-7
J1-21
XA8P1-11
J1-22
XA8P1-15
XA8P1-19
XA8P1-29
XA8P1-31
XA8P1-59
XA8P1-57
XA8P1-53
J1-29
XA8P1-47
XA8P1-25
XA9P1-66
XA9P1-34
J1-32
XA8P1-4
J1-33
C
FROM SHEET 3

EL7EO11

Figure FO-4. Circuit Card Assembly A14 Connection Diagram (Sheet 4 of 4)